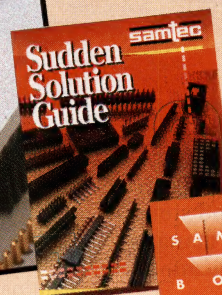


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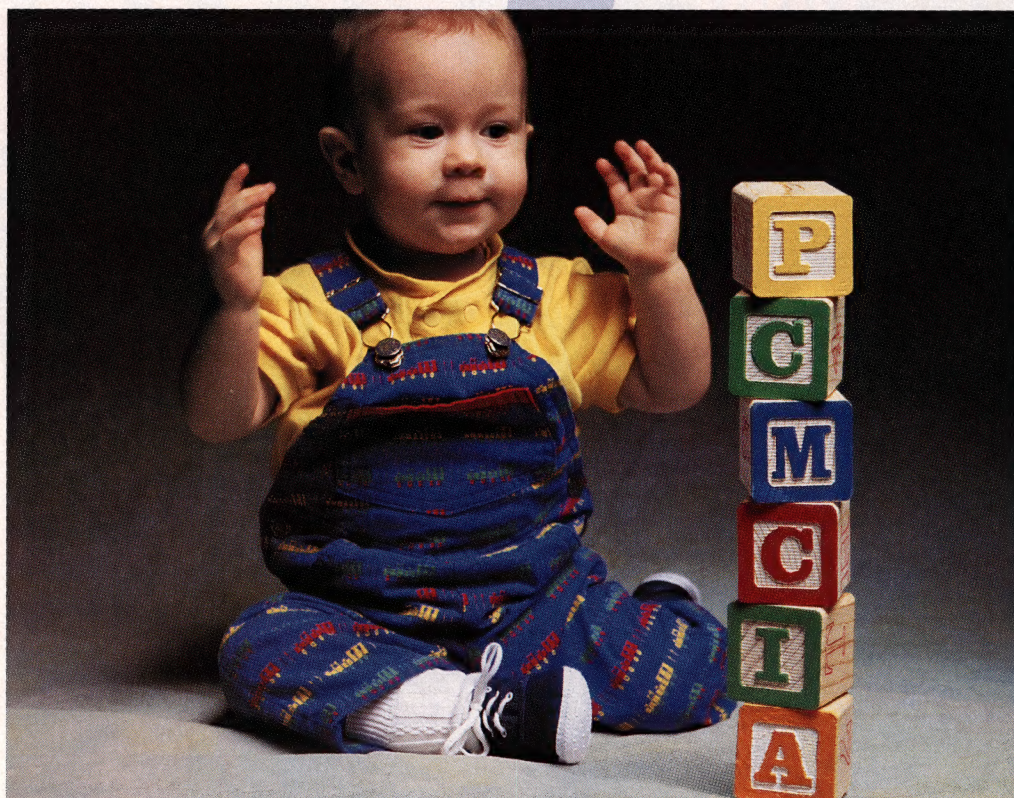
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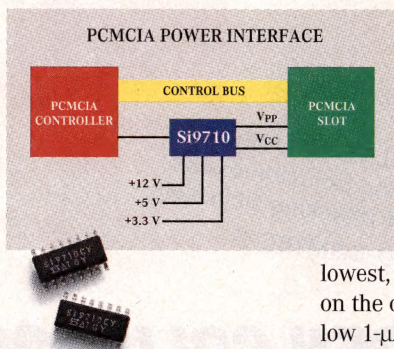
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**On the cover:** Chances are that you'll have to familiarize yourself with thermal-management techniques if you want to design high-performance systems with 32-bit microprocessors. Many approaches are available to keep products cool—it all depends on the type of project you're working on. See our Special Report beginning on pg 40. (Photo courtesy Wakefield Engineering Inc)

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## SPECIAL REPORT

### Cooling hot microprocessors

40

The latest  $\mu$ Ps have given rise to some ingenious new ways to keep systems from losing their cool. So far, though, veteran designers are waiting for proof of cost-effectiveness before warming up to these new technologies.—*Dan Strassberg, Senior Technical Editor*

## DESIGN FEATURE

### Regulator topologies standardize battery-powered systems

59

Power supplies are perhaps the most crucial elements of a battery-powered system. Knowledge of some basic regulator topologies will help you select or design the right supply configurations for your needs.—*Bruce D Moore, Maxim Integrated Products*

## DESIGN IDEAS

- |   |           |
|---|-----------|
| <b>Pulse stretcher increases ECL-gate gains</b>     | <b>73</b> |
| <b>Expanded-scale voltmeter uses just two parts</b> | <b>73</b> |
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## TECHNOLOGY UPDATES

### Teaming a logic analyzer with a debugger provides advantages to both tools 21

Logic analyzers are good for debugging embedded systems, but they're not the ultimate. Pairing them with debuggers, though, addresses many of the drawbacks of using logic analyzers alone.


—*David Shear, Technical Editor*

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John M Angelini, Beverly Blake



January 20, 1994

Continued from page 5

## TECHNOLOGY UPDATES

### Logic design is alive and well

29

Aristotle used it, George Boole boosted it, John Von Neumann named it, and it first glowingly appeared in vacuum tubes. Despite its long history, logic design is alive and well; it has become a base technology and a lingua franca for digital designers.

—Ray Weiss, *Technical Editor*

## EDITORIAL

### Project Tin Roof and EDN's EMC supplement

17

Every member of your design team should have a gut-level feel for electromagnetic-compatibility issues. The EMC supplement shipped with this issue is a tool you can use to achieve that goal.

—Steven H Leibson, *Editor-in-Chief*

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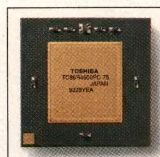
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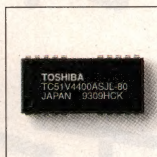
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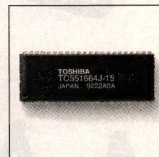
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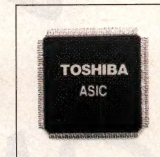
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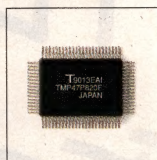
*High Speed  
SRAM*



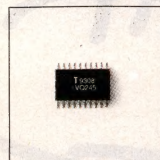
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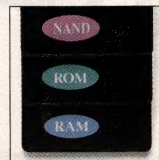
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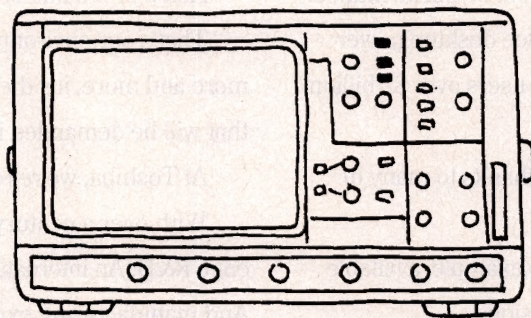
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EDITED BY FRAN GRANVILLE

## Resonant-tunneling transistors work at room temperature

At the International Electron Devices Meeting in Washington, DC, scientists at Texas Instruments demonstrated a quantum-effect IC that operates at 75°F. The company projects that the circuit, which uses the quantum-mechanical effect of resonant tunneling, operates three times faster and has three times the density of conventional ICs. In the logic circuit, which is a 1-bit full adder, resonant-tunneling bipolar transistors reside side-by-side with conventional double heterojunction bipolar transistors. The company's process that combines the two technologies allows for more efficient switching operations and more efficient logic implementation. Instead of the 40 transistors required using a conventional process, this adder comprises 17 transistors.

The key technical breakthrough in demonstrating the IC was the development of resonant-tunneling transistors with practical values of current gain, on-off current ratio, and breakdown voltage. The demonstration IC achieved a current gain as high as 100 and operated at 3V with a logic swing of 1.2V. The company fabricates the IC with compounds of indium, phosphorous, gallium, aluminum, and arsenic rather than using silicon.

Resonant tunneling permits an electron to pass through a classically impenetrable barrier under certain conditions. In this case, the transistor operates by transferring electrons from one layer of the circuit to another under the control of a voltage that is applied to a control terminal, as in a conventional transistor. However, the design of the quantum switches exploits quantum resonance in the electron motion, so that a single transistor exhibits many on and off states. This switching characteristic reduces the number of transistors needed and reduces the number and length of wires required to assemble the transistors into an IC.

The company foresees several possible near-term applications of resonant-tunneling transistors, including micro-

wave ICs, A/D converters, high-bandwidth digital video, very high-speed triggering circuits, and high-speed logic.—by Anne Watson Swager

Texas Instruments, Dallas, TX, (800) 336-5236. **Circle No. 346**

## Data Pump IC lowers T1 costs

The high-speed digital-subscriber-line (HDSL) Data Pump from Level One Communications converts two wire pairs into the equivalent of a T1 (1.544-Mbps) digital link through the telephone network. Unlike T1 links, however, Data Pump produces two bidirectional 784-kbps signals rather than a unidirectional 1.544-Mbps signal on each line.

The device tolerates a mixture of wire gauges and the presence of bridge gaps in the cabling between a user and a central office. It also transmits signals as far as 12,000 ft, compared with T1's need for repeaters every 3000 to 5000 ft. These two features allow Data Pump to establish a high-speed link over existing telephone cabling rather than requiring a special installation, thus lowering costs for high-speed data transmission.

Data Pump has reached production stage, but parts are not generally available. A telecommunications-industry consortium sponsored the part's development, and members have exclusive access to the device for a time. Later this year, the part will become available outside the consortium, and Level One will set pricing.

—by Richard A Quinnell

Level One Communications Inc, Folsom, CA. (916) 985-3670.

**Circle No. 347**

## ASIC/software combo speeds laser printers

By tackling the job of converting graphics commands into raster data, Destiny Technology's WinStyler software and ASIC help lower the cost of laser printers and speed printing. The

## SHORTS

**Virtual prototype employs StereoGraphics' eyewear.** Lockheed Research Labs, Palo Alto, CA, has announced an optomechanical virtual prototype, developed entirely in virtual reality, that uses StereoGraphics' CrystalEyes LCD eyewear. Lockheed used the prototype for the NASA/Goddard December 1993 service mission to the orbiting Hubble Space Telescope. The prototype enabled scientists to test the deployment of the COSTAR (Corrective Optics for the Space Telescope Axial Replacement) assembly without developing physical prototypes or models. CrystalEyes enabled scientists to view the full-color, 3-D COSTAR in stereo depth. StereoGraphics, San Rafael, CA, (415) 459-4500.

**Circle No. 350**

**Largest collection of historical mil specs now on CD-ROM.** Information Handling Services has placed its collection of unclassified, canceled, and superseded US military standards, specifications, drawings, and related documents on CD-ROM. The documents provide PC users with access to full-text images of documents that are vital to maintaining, repairing, and modifying military equipment. Information Handling Services, Englewood, CO, (800) 241-7824.

**Circle No. 351**

**M-Systems forms alliance with Maxtor.** Flash-disk memory manufacturer M-Systems has announced a strategic alliance with mass-storage-device manufacturer Maxtor Corp to develop flash-memory-based, PCMCIA-compatible storage products for the mobile-computer market. M-Systems, Fremont, CA, (510) 505-9081.

**Circle No. 352**



## SHORTS

**NTIS offers federal-resources guide.** The National Technical Information Service of the US Department of Commerce is offering the fifth edition of its *Directory of Federal Laboratory & Technology Resources: A Guide to Services, Facilities, and Expertise*. The 736-pg publication lists resources, including contact names and phone numbers, of government labs, research centers, testing facilities, and technology-information centers. \$65, plus \$3 shipping; order no. PB93-1000097KSZ. National Technical Information Service, Springfield, VA, (800) 553-6847. **Circle No. 353**

**High-tech humor.** Oak Ridge Public Relations has announced the publication of *The First, Advanced, State-of-the-Art, High-Performance, Totally Integrated, Revolutionary, Leading-Edge, High-Tech Joke Book*. The 210-pg volume offers a collection of humor on technology, computers, software, science, and mathematics. Available at retail book stores or from Oak Ridge for \$14.95, including shipping. Price in California is \$17.81. Oak Ridge Public Relations Inc, Cupertino, CA, (408) 252-5042. **Circle No. 354**

**IBM renames division.** IBM Corp has renamed its Workstations and Systems Division; the new name is the IBM RISC System/6000 Division. IBM Corp, White Plains, NY, (914) 642-5463. **Circle No. 355**

**Resource guide covers embedded-PC standard and products.** The PC/104 Consortium has published the fourth edition of its *PC/104 Resource Guide*. The 120-pg booklet, which is free to engineers and companies developing embedded systems, offers an overview of the PC/104 standard, a cross-reference of related products and functions, and product listings from more than 75 of the consortium's member com-

panies describing their PC/104 modules and other related boards, peripherals, and software. PC/104 Consortium, Sunnyvale, CA, (408) 245-9348. **Circle No. 356**

**Teradyne wins ARPA boundary-scan contract.** E-Systems Inc of Greenville, TX, has awarded Teradyne a 2-year, \$1.5-million contract to develop boundary-scan design and test tools for the Defense Department's Advanced Research Projects Agency application-specific electronic module (ASEM) multichip-module program. Under the contract, Teradyne will extend its Victory boundary-scan test software to enable Victory test programs and diagnostics to work with a variety of other commercially available automatic test equipment. Teradyne Inc, Boston, MA, (617) 482-2700. **Circle No. 357**

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**EIA is available on line.** You can now access press releases, product information, and other materials from the Electronic Industries Association (EIA) and EIA-member companies through the CompuServe online information service. EIA, Washington, DC, (202) 457-8700. **Circle No. 359**

software uses the host CPU's spare processing power to handle the conversion then sends the printer data in raster format. The ASIC provides a bidirectional link to the printer along with data compression to increase the effective data bandwidth.

WinStyler aims to eliminate the need for laser printers to have powerful controllers and large amounts of memory to handle the rasterization of graphics commands. By moving that effort to the host computer, WinStyler also allows users to upgrade their printing capabilities with a software change. Further, the print function's speed increases as the host system upgrades without changes to the printer. Printers using WinStyler should offer 600-dpi resolution at a retail price of less than \$750.

—by Richard A Quinnell

Destiny Technology, Santa Clara, CA, (408) 562-1000. **Circle No. 348**

## Control-engineering expo slated for mid-March

The third annual International Control Engineering (ICE) Exposition & Conference takes place March 14 to 17, 1994, at McCormick Place North in Chicago. The conference focuses on using control technologies to improve productivity, quality, and communications in discrete and process manufacturing.

The exposition highlights products that result from manufacturers' applying discrete- and process-control technologies in motion-control systems, PLCs, actuators, displays, transducers, relays, data-acquisition devices, and measurement devices.

Conference seminars will address the challenges that users, designers, and managers face when implementing control technologies, such as creating manufacturing-execution systems and rapid prototyping, managing product information, and integrating the factory floor with front- and back-end operations. Representatives from companies such as Motorola and Intel will chair these seminars.

—by Jim Leonard

Reed Exhibition Companies, Stamford, CT, (203) 352-8297. **Circle No. 349**



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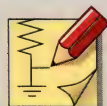
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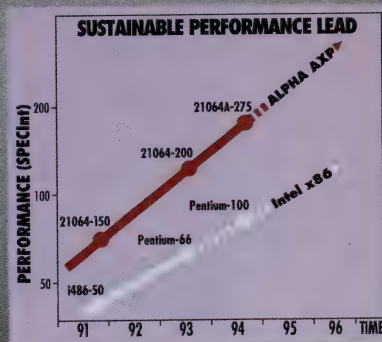
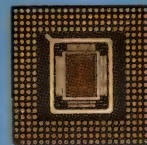
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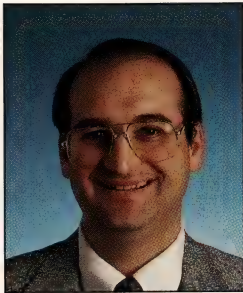
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# Project Tin Roof and EDN's EMC supplement



It was 1978, and electromagnetic-compatibility (EMC) issues were biting us at Hewlett-Packard's Desktop Computer Division. Three years before IBM would introduce its PC, our development group in the Colorado foothills owned the desktop-computer market with the 9825 and 9845 desktop computers. Users could buy a variety of interface cards for these machines—and there lay the problem. The cards' I/O cables made our computers more susceptible to electrostatic discharge, and they spewed electromagnetic interference (EMI) into the ether. According to our EMC test engineers, it was only a matter of time before the FCC came knocking. I managed a crash project to solve the I/O cables' EMC problems. We named the project "Tin Roof," referring to expected solutions involving metal shielding and with more than a nod to Tennessee Williams' *"Cat On a Hot Tin Roof."*

Lacking practical EMC knowledge hampered our efforts. Back then, we didn't fully understand the sources of EMI or the coupling mechanisms that allowed noise sources to escape the computer. Worse, we had very poor understanding of the EMC aspects of "ground." Existing literature didn't help much. Most of the information published on EMC was either geared toward the military or was too esoteric to give us a gut feel for the problem's practical characteristics.

As with any after-the-fact EMC project,

Tin Roof had to adopt a "Band-Aid" approach. The I/O cards were already on the market, as were the desktop computers. Cases, form factors, and prices were already in place. The solution we developed had to retrofit into these existing parameters. Ultimately, we zeroed-in on the I/O cards' grounding system and developed a die-cast card housing that clamped the I/O cable's shield braid and grounded to the desktop computer through a large contact spring. This new grounding scheme replaced one formed by a mixture of the cable-shield's drain wire, 20-mil pc-board traces, and several connectors.

Today, anyone with a good feel for EMC design techniques would double over laughing at our original grounding scheme; but back then, we just didn't understand. We had to develop the necessary EMC knowledge on our own.

Now, 15 years later, many of you are still looking for good, practical help with EMC issues. That's why I'm pleased to present you the finest introduction to EMC design that I've seen. Bill Kimmel and Daryl Gerke, two successful EMC consultants, have captured critical design information you'll need to tame EMC problems. Their "Designer's Guide to Electromagnetic Compatibility" is a clear, comprehensive, and easy-to-read supplement you'll find packaged with this issue of EDN.



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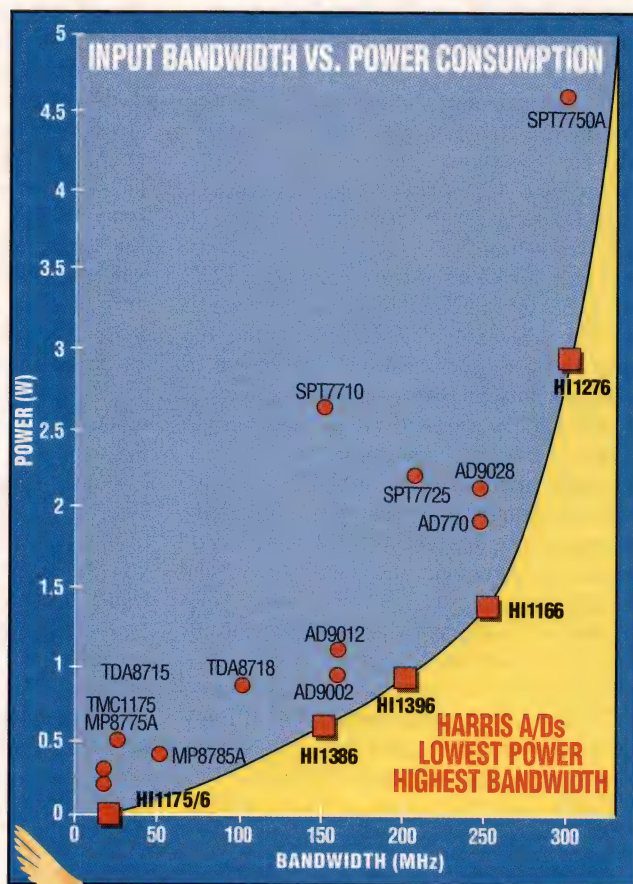
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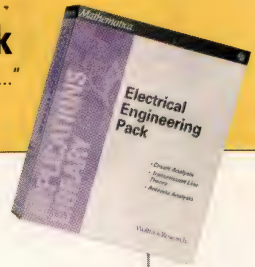


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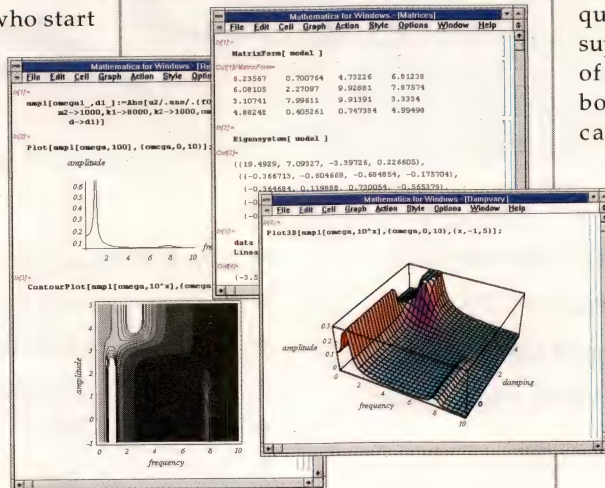
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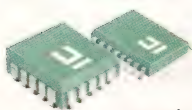
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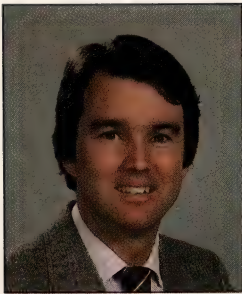
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# Teaming a logic analyzer with a debugger provides advantages to both tools

DAVID SHEAR, Technical Editor



**Logic analyzers are good for debugging embedded systems, but they're not the ultimate. Pairing them with debuggers, though, addresses many of the drawbacks of using logic analyzers alone.**

You might think of a logic analyzer as a tool for misguided hardware engineers who want to play with ones and zeros. They use logic analyzers to gleefully connect what seem to be thousands of probes on the target. Then they stare, wide-eyed, at a display full of random numbers or strange lines.

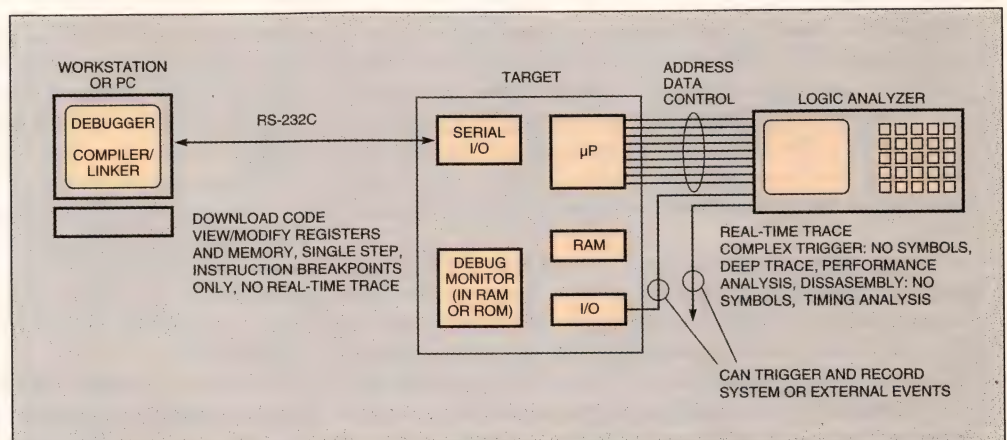
As a software engineer, you most likely stay away from logic analyzers. Your world exists in a high-level language (HLL), probably C. You are most comfortable in front of your workstation or PC debugging your code by setting breakpoints, single-stepping, and watching variables change. Even if you are programming in assembly language, you are most likely more comfortable using a debugger that lets you refer to your program via symbols.

Despite these prejudices, you can get some real advantages from a logic analyzer, but it is not the ultimate debugging tool. No single tool can solve all possible problems; each has its strengths and weaknesses (see box, "Pros and cons of using logic analyzers to debug embedded systems"). Using a

debugger along with a logic analyzer, however, addresses many of the problems of logic analyzers.

When you use a logic analyzer alone (Fig 1), it acts primarily as a recording device that records what a target does. As such, it allows you to look at the recording and see what happened. The logic analyzer also allows you to go beyond the  $\mu$ P and trigger on-system events or even events external to the system you are debugging. For example, you can trigger a logic analyzer when a certain pattern shows up on a parallel interface, or you can set the trigger on a contact closure outside the target's box.

A trigger to a logic analyzer is similar to a breakpoint in a debugger. When inputs to the logic analyzer meet certain trigger parameters (trigger qualifiers), the logic analyzer performs a task. In most cases, the task is to fill up the trace buffer with program-execution data. In some cases, the logic analyzer's trigger system might perform a single task each time the inputs meet the trigger conditions. For example, the logic analyzer may record only the data written into a vari-



**Fig 1—A logic analyzer and a debugger alone provide many useful debugging functions. Unfortunately, they don't take advantage of what each tool offers.**



## LOGIC ANALYZERS/DEBUGGERS

able. As a result, the logic analyzer records the many—perhaps millions of—times your program changes that variable. You can then see which functions within your program affect the value of the variable.

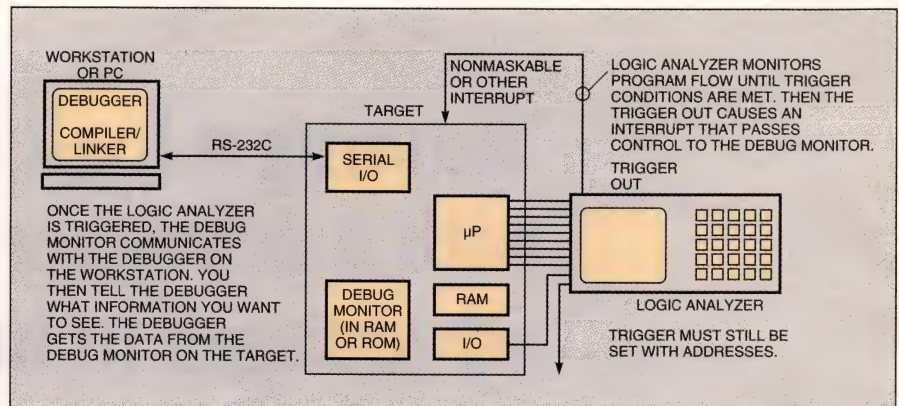
**μP pods reduce cable clutter**

Most logic analyzers also have optional μP pods that connect directly to the target. These pods replace the mass of probes with a single rather large connector. All the important signals from the μP go to the logic analyzer through this one pod.

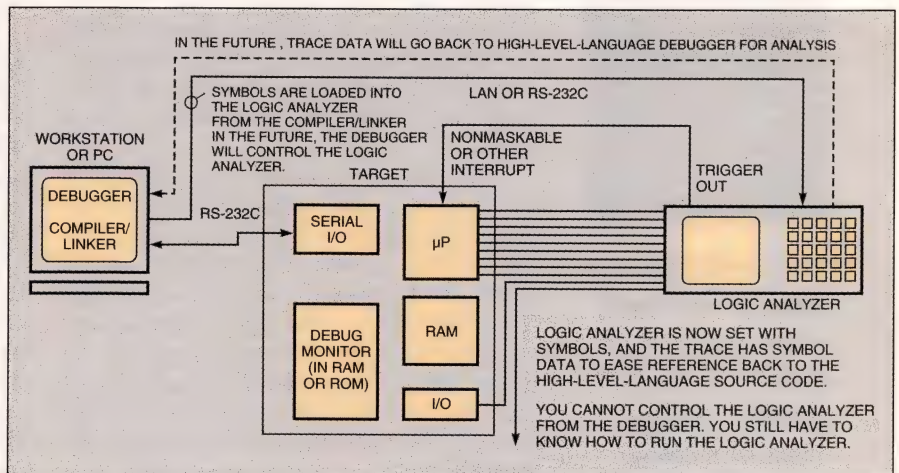
Another common option on logic analyzers is a disassembler, or an inverse assembler, a software option that works within the logic analyzer to convert the acquired data in its trace buffer into assembly-language mnemonics. This option lets you view the assembly-language instructions instead of looking at logic levels.

Although you can use a logic analyzer alone, you could alternatively use it with a debugger. Using a debugger running on a workstation along with a debug monitor running on a target allows you to download a program and debug it as it runs on the target. The debug monitor, often called a ROM monitor, usually resides in ROM but can also reside in RAM.

The debug monitor controls the operation of the target by replacing instructions in the target's program memory with breakpoint instructions. The breakpoint instruction stops your tar-



**Fig 2—Using the trigger output of the logic analyzer to break the target program provides much better breakpoint options. Once the logic analyzer is triggered, the debug monitor communicates with the debugger on the workstation. You then tell the debugger what information you want to see.**



**Fig 3—Without symbols, it is difficult to set up the logic analyzer. Let the output of your compiler/linker give the logic analyzer the information to allow you to set it up with the symbols from your program. In the future, the debugger will control the logic analyzer, and trace data will go back to the high-level-language debugger for analysis.**

## Looking ahead

The ideal future would allow you to use a debugger on your workstation or PC without regard to the type of tool connected to the target. If using a logic analyzer, you would pull down menus and select options for triggering the logic analyzer from the debugger. You would then bring the trace data from the logic analyzer to the debugger. The trace data would then be presented in your high-level language (HLL).

For the next year, you will still have to learn how a logic analyzer works before you can use one. Because there are so many logic analyzers and debuggers available, it will be some time before you will be able to set up a logic analyzer from a menu on a debugger. The number of commands that the debugger must be able to interpret to control one logic-analyzer family—let alone many of them—is not trivial.

The ability for a debugger to analyze trace memory and

automatically refer it to the source code is even further off. The best debuggers currently available let you place source-code symbols in the trace data.

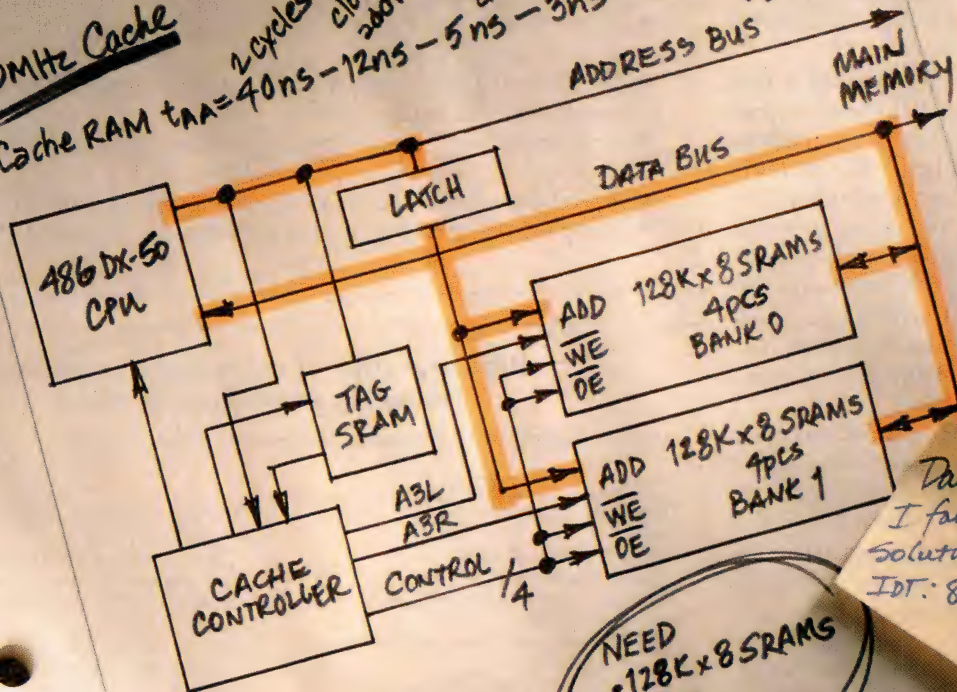
The dashed line from the logic analyzer to the workstation in **Fig 3** represents a link that does not yet exist. However, in the future, the trace data will go back to the debugger, and you will be able to "walk through" the trace buffer in HLL source code. This ability will be like walking through a listing, except that it will enable you to see exactly what your program did on the target while the logic analyzer recorded data. It also will let you see when each instruction on the target was executed.

During the next year, new products will mostly be "convenience" products—those that allow you to buy all the tools from one source or that allow you to simplify some complex steps in debugging an embedded system.



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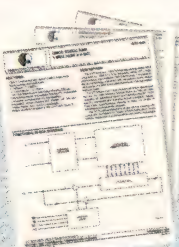
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## LOGIC ANALYZERS/DEBUGGERS

get program and gives control to the monitor. The monitor then communicates with the debugger on the PC or workstation and allows you to perform debug operations. You can set a breakpoint only on an instruction, not on memory access. For example, you cannot set a breakpoint when a variable changes.

If you merge a logic analyzer with a debugger (see **Fig 2**), then you can take advantage of the very complex triggering capabilities of the logic analyzer. You can set a breakpoint on almost anything, including memory accesses, so that you can determine such things as which functions are modifying a global variable or which function is corrupting your stack. Or you can cause a debugger breakpoint on system events.

Unfortunately, to do this, you must set up the breakpoint conditions on the logic analyzer, which means that you have not only to learn how to use the logic analyzer but also to figure out the absolute address of all the functions and variables of interest.

### Symbols are more than symbolic

To make logic analyzers easier to use, many of them now accept symbols from compiler/linkers (see **Fig 3**). Once you load the symbols into the logic analyzer, you can use the symbols to set triggers. The symbols also let you easily reference the trace data to an HLL source. You can send thousands of symbols to the logic analyzer. In many cases, you can

## System restrictions to using logic analyzers

You cannot use the logic analyzer/ debugger approach on all systems; you can use it only on those systems with the following features:

- Enough onboard RAM to run the program (however, you can overcome this restriction by having the program reside in a ROM emulator)
- Space in RAM or ROM for an in-circuit debug monitor and a target program
- A spare serial I/O port
- NMI (nonmaskable interrupt) or other interrupt available to trigger the debug monitor from the logic analyzer
- A connector or a test point to connect the trigger from the logic analyzer to the target
- A level converter for the trigger to interrupt the signal on the  $\mu$ P
- Enough space to connect the logic analyzer's probes or pod

## Pros and cons of using logic analyzers to debug embedded systems

Logic analyzers have the following pros and cons. They:

Pros	Cons
Are least intrusive	Cannot look inside the $\mu$ P to see internal RAM or ROM
Provide real-time trace	Cannot monitor on-chip cache
Trigger beyond the processor	Can cause a tangle of wiring
Provide trigger qualifiers to store complex data	Must debug high-level language in assembly language
Provide deep trace (large memory to record data)	Do not provide control of the target (no breakpoints)*
Can look inside the $\mu$ P cycle to see bus timing	Cannot modify registers or memory*
Can investigate timing to external real-time events (time from the external event to the interrupt response)	Cannot download code*
Provide time-stamping of all events	
Provide performance analysis	
Do not affect timing of target (do not slow it down)	
Are indispensable for getting a complex design running	

\*Logic analyzers can overcome these drawbacks when you use them with debuggers.

## For free information...

For free information on the logic analyzers useful in debugging embedded systems, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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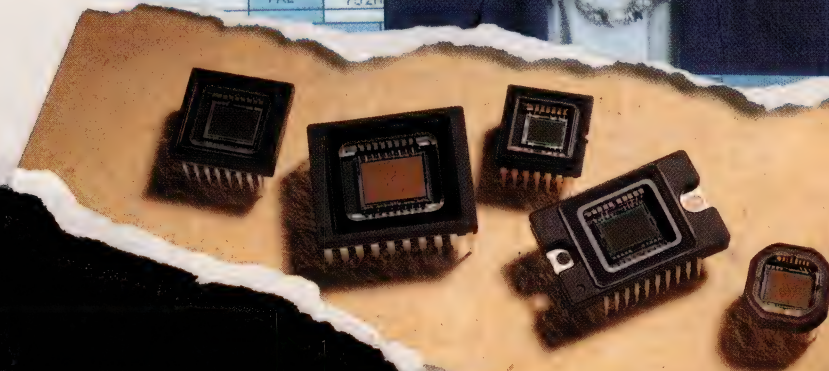
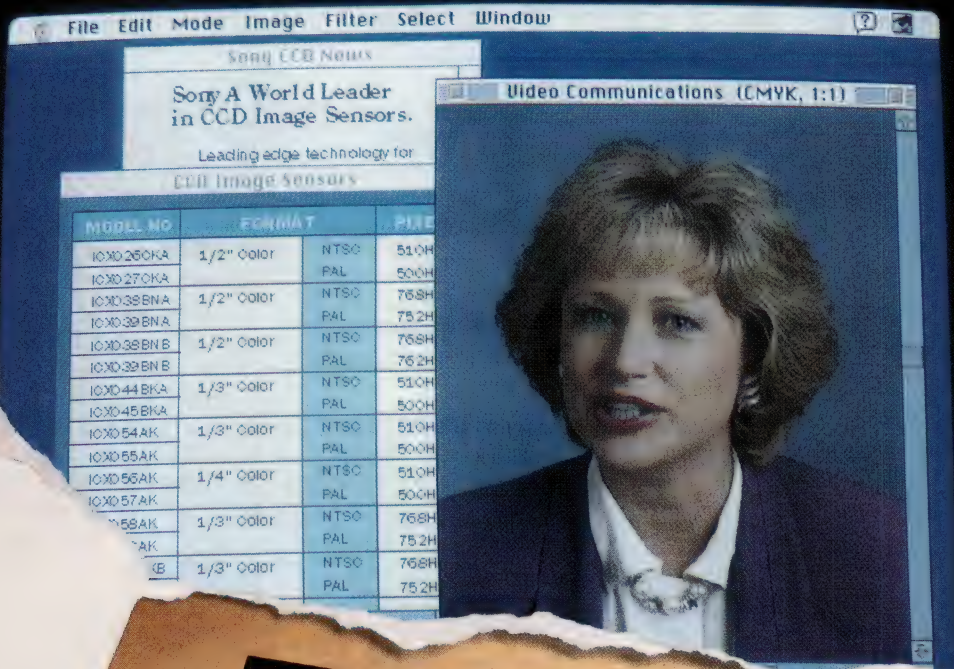


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## EDN-TECHNOLOGY UPDATE

### LOGIC ANALYZERS/DEBUGGERS

send even the line numbers of your source code as symbols. This technique allows you to easily set breakpoints on HLL statements and refer the data in the trace buffer back to the HLL code.

Also in Fig 3, only symbols—not setup commands—go from the workstation to the logic analyzer. You cannot set triggers on the logic analyzer from within the debugger. This means you have to understand how to use the logic analyzer and often must leave your workstation and go to the logic analyzer to set it up.

### Put all the tools on a screen

However, some logic analyzers, such as the Enterprise DAS from Tektronix, let you use the logic analyzer as a separate tool but provide the convenience of having all the tools on your workstation screen. Enterprise works with X Windows, which means that if you are also running other tools under X Windows, you can set up a separate window for the debugger, the compiler/linker, and the logic analyzer. This makes it much easier to control the tools and reference the data acquired by the logic analyzer to your HLL source code.

Logic analyzers are not the perfect instrument; other approaches, such as in-circuit emulation, are more appropriate at times. But logic analyzers are very powerful tools for debugging embedded systems, especially when combined with debuggers. As they become more integrated with debuggers, their usefulness to software debugging will increase. **EDN**

Technical Editor David Shear can be reached at (503) 754-9310, fax (503) 758-9242, Internet: ednshear@mci-mail.com.

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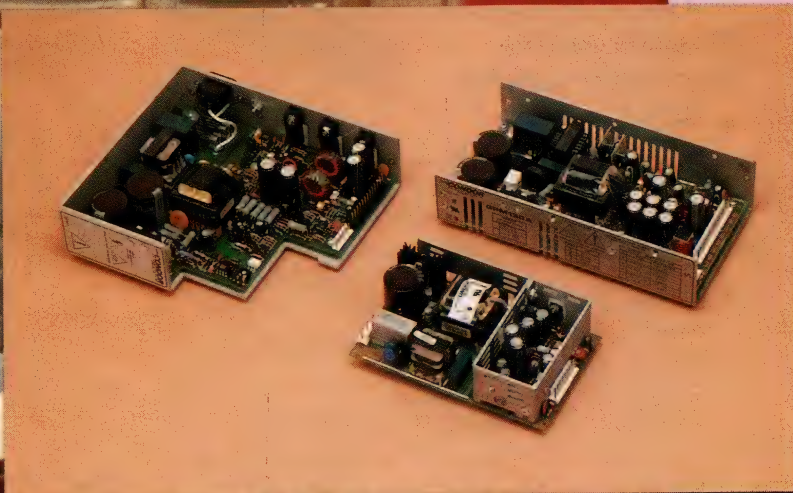


For practical help with issues involving EMC (electromagnetic compatibility), take a look at our "Designer's Guide to Electromagnetic Compatibility," packaged with this issue of EDN.



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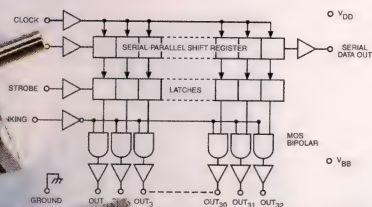


# CURRENT SHOWCASE

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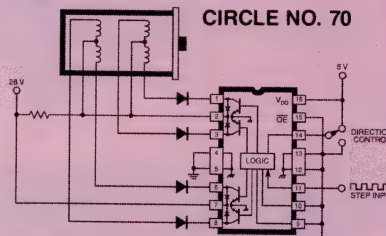


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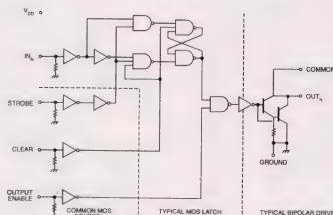


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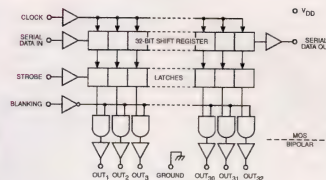


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## BiMOS II 32-Bit Serial-Input, Latched Drivers — 5832

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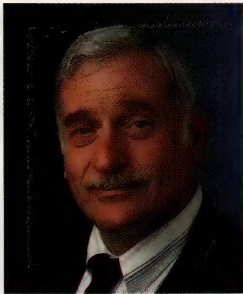
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# Logic design is alive and well

RAY WEISS, Technical Editor



**Aristotle used it, George Boole boosted it, John Von Neumann named it, and it first glowingly appeared in vacuum tubes. Despite its long history, logic design is alive and well; it has become a base technology and a lingua franca for digital designers.**

Logic design is here to stay. The Boolean equations and Karnaugh maps we learned in school still work, enabling us to map design concepts into working silicon. Like the programmers before them, engineers are learning to deal with a lack of certainty as our designs map down through a software-synthesis layer to an implementation. The equations or gates you write, even for PALs, can take on a different, optimized form.

However, logic synthesis has emerged as a core design technology for system and board designers. ASIC designers rely on synthesis to provide a level of technology (and foundry) independence as well as a mechanism for higher level design above gates and layout. Current synthesis technology supports synthesis and optimization for combinatorial logic, data-path element generation, and simple state-machine design and synthesis.

Designers are now applying synthesis technology to programmable logic, mainly FPGAs and CPLDs. These chips are highly layout dependent, and FPGA synthesis has not yet reached ASIC effectiveness. Major synthesis-tool vendors, such as Synopsys, have FPGA tool compilers. Additionally, Cypress and Data I/O have VHDL (VHSIC Hardware Description Language)-based synthesis tools for PALs and PLDs. Some designers are mixing technologies, doing top-down, HDL-based designs and then synthesizing the logic into a mixture of ASICs and FPGAs.

Logic design still has a long way to go, according to some practitioners. Still lacking are tools for design verification and design debugging. Instead, logic and system designers are left to their own devices to figure out how to test their prototype circuits. Currently, no at-speed, logic-debug support systems comparable to those available to embedded system developers are available; nor are logic ICEs or special bond-out chips

available that show what your circuits are doing within the chip while running in situ, in the system. You can indeed simulate your designs, but simulation is not enough for many designers who also want real-time, in-system emulation. Large, reduced-speed logic emulators (such as Quickturn's) are available.

And finally, a new twist is emerging for programmable logic: dynamic reprogrammability. You can view RAM-based FPGAs and CPLDs in the same light as microprocessors with RAM or flash memory; the executing logic or software machine can be loaded periodically for different tasks.

Today, some engineers reload FPGA logic functions mainly to perform off-line testing. A few designers are dynamically reloading their logic to perform different logic functions over time. Others are experimenting with so-called "soft computers," which dynamically map new and different CPU architectures on pro-

grammable logic to match application and algorithm demands.

Today's engineers crank out designs in representations ranging from logic schematic to PAL equations or HDL descriptions in VHDL or Verilog, all incorporating logic fundamentals. Such logic representations are accepted as a solid base for design, having easily understood elements such as logic gates, multiplexers, ALUs, multipliers, flip-flops, registers, counters, and memories.

By highlighting different realities in the bustling world of design, four designers offer their views on the current state of technology (see **boxes** starting on pg 30). Each designer represents a range of experience, from small ICEs to large communication systems, from discrete and PAL-based design to simulation and top-down HDL design.

**Designers are now applying synthesis technology to programmable logic, mainly FPGAs and CPLDs.**

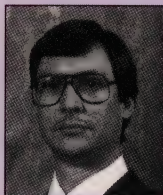
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## LOGIC-SYNTHESIS DESIGN

**Randall Huddleston**, VP of Engineering, Integrated Business Computers, Chatsworth, CA.

*IBC fields a Unix-based server system. Still a hands-on designer, Randy recently developed IBC's Pentium module for mother-board designers. The PentiCache module incorporates a Pentium  $\mu$ P, a cache subsystem (Intel cache controller), and a system bus for multiple PentiCache modules that share a common main memory.*



"Logic design itself is fairly easy; the problems arise in juggling faster clock speeds and in dealing with packaging, layout, and timing. Clock rates for processors such as the Pentium are 66 MHz—and will be going even higher. Many companies don't have the expertise to design

wide bus systems that run at these clock rates, which is why we created the Pentium module. You have to worry about board layout and transmission-line effects. We actually have a consultant, a microwave-amplifier board designer in our building, who helps us out with these issues.

"With higher clock rates, you need to pay more attention to setup, hold, and timing margins. You must also pay careful attention to chip-vendor signal constraints. If Intel specs 250-nsec signal skews, it means 250-nsec skews—you cannot ignore it. We actually use filters in

front of our logic to eliminate metastability problems. These filters are fairly complex logic and are used to filter out transient noise that precedes the critical clock and signal edges.

"On the output side, we've found that EPLDs can be unpredictable when an internal flip-flop signal drives a heavily loaded external pin. The signal can oscillate and have degraded rise and fall times. We've found it better to use a gate or a combinatorial output to drive external signals. Sure, you gain a gate delay, but you more than make it up in better signal rise and fall times.

"We generally use EPLDs (from Altera or Intel) and PALs for design. We have done a gate array, transferring EPLD designs into an ASIC. Because gate arrays tend to be pin limited, we actually put four designs into a single gate array and used input parameters to select the dominant logic subset. The chip worked without needing fixes."

**Alex Kolchinsky**, President, Dynamic ReSolutions, Andover, MA.

*Alex Kolchinsky was Chief Engineer for the digital-imaging group at Analogic Corp (Peabody, MA), where he developed techniques for dynamically reconfiguring core logic (FPGAs) in image-processing systems. Using these techniques, the hardware could be optimized—in effect, tailored—for each algorithm stage; the techniques led to minimal designs with high processing efficiencies and typical cost reductions on the order of 4×. Alex has two patents pending, one entered jointly with Analogic. In 1993, Alex started Dynamic ReSolutions, a system design house aimed at providing dynamic reconfigurability for embedded OEM products.*




"The image-processing market of the 90s is changing too rapidly to allow developers to spend 12 months or more creating custom hardware for imaging systems. That's just too long for many products. Moreover, standard programmable designs are still very expensive; costs to an OEM customer generally start at \$5000 for a board and \$30,000 for a system.

"Using current technology, a designer creates a full design with multiple modules, with each module optimized for a specific processing function. A cheaper option is to optimize logic in time, not just space. Instead of dedicating logic to each function, the logic can be 'time-shared'; it can be configured over time as a function of algorithmic requirements. For example, using SRAM-based FPGAs, an image processor can modify its ALU logic, adding adders, multipliers, and barrel shifters as needed. The controlling state machines can be modified as well. Using this time-share technique minimizes logic,

cuts power consumption, minimizes bus requirements, and increases processing power. Even better, you end up with a common design base that can be configured for different applications. Thus, you get an off-the-shelf platform with the advantages of custom design.

"A reconfigurable design builds on core programmable logic (SRAM-based FPGAs), supplemented by memory to hold multiple configurations and data, and a control processor that directs execution and reconfiguration. The best development methodology for such a system is to analyze and develop your algorithms on a standard software-programmable platform. When the algorithms are stable, you can map them into a reconfigurable hardware system to cost optimize for maximum throughput with minimum costs. We use Xilinx FPGAs and partition our designs into multiple chips. Current FPGA technology lends itself to reconfiguration at natural process breaks or algorithm stages."





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## LOGIC-SYNTHESIS DESIGN

### For free information...

For free information on the logic-synthesis products discussed in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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**Advanced Microcomputer Systems Inc**  
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CAE tools (CUPL)  
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**Altera Corp**  
San Jose, CA  
(408) 894-7000  
CPLDs, CAE tools  
Circle No. 439

**Advanced Micro Devices**  
Santa Clara, CA  
(800) 222-9323  
PALs, CPLDs, CAE tools  
Circle No. 440

**Atmel**  
San Jose, CA  
(408) 436-4333  
FPGAs, CAE tools  
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**AT&T**  
Allentown, PA  
(800) 372-2447  
FPGAs, CAE tools  
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**Cadence Design Systems Inc**  
Santa Clara, CA  
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HDL, synthesis CAE tools  
Circle No. 443

**Cypress Semiconductor**  
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PALs, CPLDs, FPGAs, CAE tools  
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**Data I/O Corp**  
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Programmers, CAE tools (ABEL, VHDL)  
Circle No. 445

**Exemplar**  
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PLD synthesis, CAE tools  
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**Intel Corp**  
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CPLDs, CAE tools  
Circle No. 447

**Lattice Semiconductor Corp**  
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**Mentor Graphics Corp**  
Wilsonville, OR  
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HDL, synthesis CAE tools  
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**National Semiconductor**  
Santa Clara, CA  
(800) 272-9959  
PALs, CAE tools  
Circle No. 450

**Philips Semiconductors**  
Santa Clara, CA  
(800) 447-1500  
PALs  
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**Quad Design Technology**  
Camarillo, CA  
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Timing/signal/transmission-line tools  
Circle No. 452

**Quicklogic**  
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**Synopsys**  
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HDL, synthesis CAE tools  
Circle No. 454

**Texas Instruments**  
Dallas, TX  
(800) 477-8974  
PALs, FPGAs, CAE tools  
Circle No. 455

**Viewlogic Systems Inc**  
Marlborough, MA  
(508) 480-0881  
HDL, synthesis CAE tools  
Circle No. 456

**Xilinx Inc**  
San Jose, CA  
(408) 879-4556  
FPGA, CAE tool vendor  
Circle No. 457

### Super Circle Number

For more information on logic-synthesis products available from all of the vendors listed in this box, you need circle only one number on the postage-paid reader service card.

**Circle No. 458**

## John McCool, VP of Engineering, Synoptics Communications Inc, Santa Clara, CA.

*Synoptics builds a range of communications systems for enterprise wide networks. It integrates a number of communications protocols, including Ethernet and WANs, into a network fabric. Synoptics' systems use standard 8- to 32-bit  $\mu$ Ps or  $\mu$ Cs for network control but rely on hard logic to handle the main communication interfaces and bit-stream processing.*



"It seems as if we managed to cut design time using synthesis and simulator tools, but all the other work we have to do for a product now takes more time. These tasks include getting tools to work and integrating the synthesis tools with back-end software and the

silicon vendors.

"Networks are highly unpredictable, and our hardware must handle a number of asynchronous hardware events. We use state machines to control the hardware, with multiple levels to control complexity. Our state machines can go down two or three levels. Using synthesis, we've done state machines with up to 64 states. Even with such tools, we've found that designers need to understand the state machine and what it does.

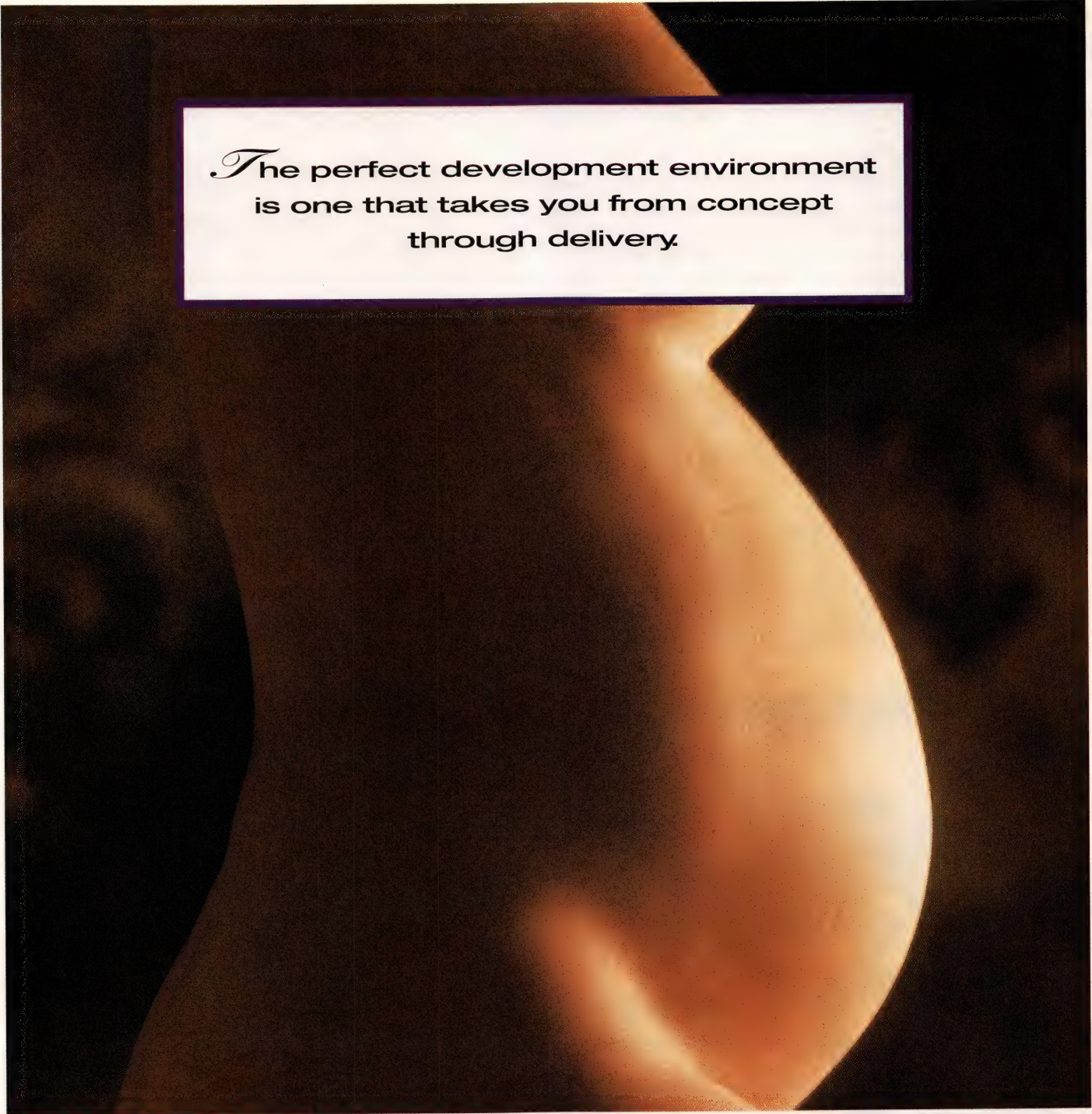
"We use PALs, FPGAs, and ASICs. PALs are the easiest to design; ASICs are straightforward but time-con-

suming: You have to get them right and do a lot of simulation. FPGAs fit in between the two. We handle FPGA designs the same as ASICs. We do top-down design, simulating at the RTL level. We separate ASICs and FPGAs when mapping the design onto hardware. Thus, we can easily retarget FPGAs to ASICs later.

"We design with VHDL. Using an HDL has proved no problem—most of our engineers knew VHDL or Verilog. Synthesis with VHDL has worked well, but to get optimum results, check to see what the tools do well and don't do well. Working with VHDL takes on aspects of a software-development environment. Engineers, however, must still remember logic basics, including clocking, edge constraints, and layout needs. Verification tools are necessary to ensure that logic meets both customer and good-design requirements, asking if it does what it should do and if it meets timing constraints and read/write edges."

Text continued on pg 34





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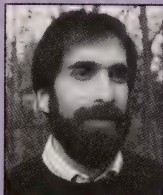
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## LOGIC-SYNTHESIS DESIGN

**Craig Haller**, VP of Engineering, P&E Microcomputer Systems Inc, Boston, MA.

*P&E supplies development environments and specialized, low-cost ICEs for a number of  $\mu$ Cs, including Motorola's 8- and 16-bit  $\mu$ Cs (Motorola also distributes P&E's tools). P&E develops small board systems. For example, the In-Circuit Debugger for the 16-bit Motorola 68HC16 fits into an RS-232C shell and uses the chip's background mode for debugging.*



"Building small board systems is easy, and it's no problem to get the boards built; the basic problem is in design, in turning in a small, efficient design in as short a time as possible. We do both hardware and software development. And that gives us a different perspective on hardware design: It's pretty apparent that the hardware tools lag behind available software.

"For starters, there's no provision for actual in-circuit debugging. Instead, CAE tools rely on simulation, rather than seeing what the actual circuit does at speed in the design. No equivalent to the  $\mu$ C in-circuit-emulator (ICE) exists. With discrete logic, I make do with a logic analyzer and a scope, but with programmable logic, especially in complex, asynchronous designs, things get much tougher.

"Today, hardware design is roughly where  $\mu$ C-application design was back in the 70s, when very few tools for debugging code were available—you were on your own.

Even the 8049 had a pin for single stepping the CPU clock. There are no similar 'features' or 'assists' for debugging programmable logic. You have to do your own debug logic, which takes up silicon.

"Also, hardware-development-tool vendors seem to have forgotten about the small companies, the garage-shop operations that gross under \$1 million a year. Tools such as those for programmable logic are expensive and, in many cases, are restricted to vendor-specific architectures. Small companies can't afford to spend thousands of dollars for tools to evaluate an architecture they may or may not use. (There are exceptions, however, such as Intel, which offers a free package and PLDshell for its CPLDs). I am working on a new ICE that uses 20 discretes—or four chips if I use PLDs. The temptation is to continue to use discretes because all you need is a schematic and standard lab tools. PALs are pretty easy to check unless you're doing complex, asynchronous logic, which can take a few passes to get right."

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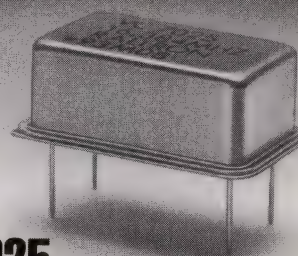
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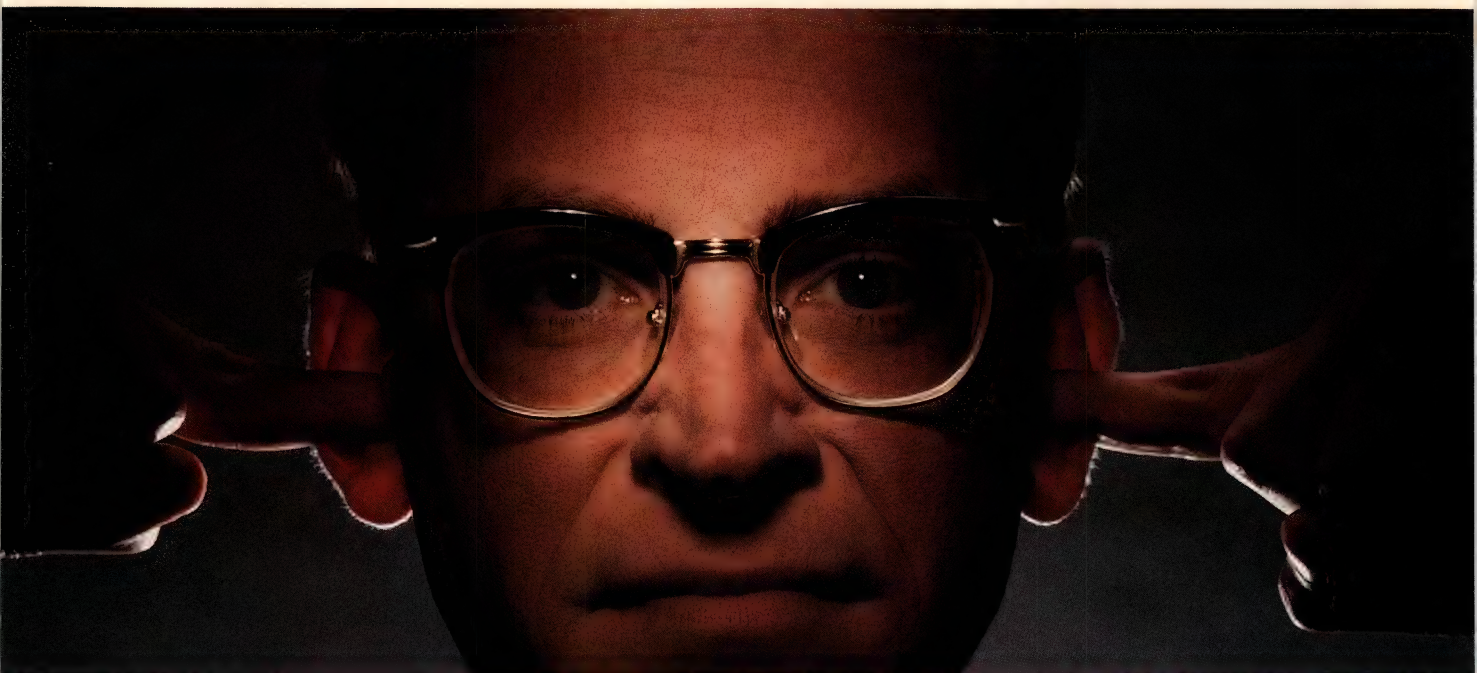
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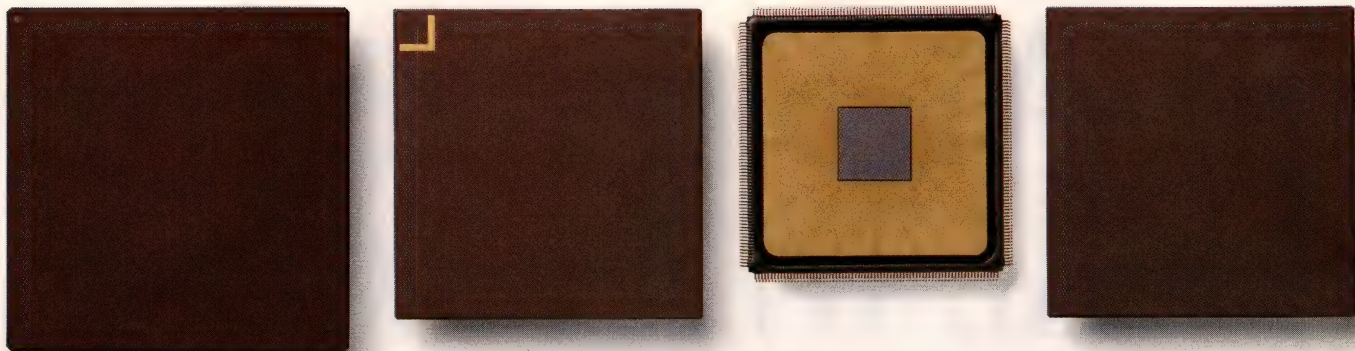


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# Burners.

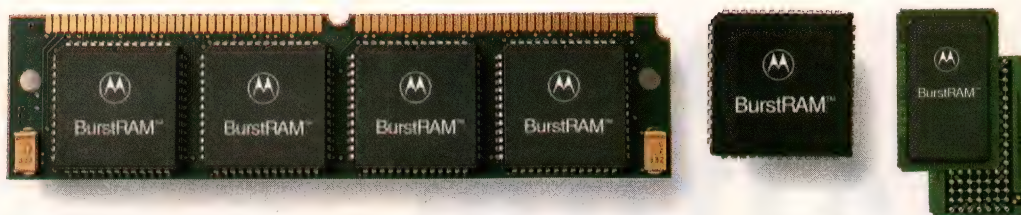
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# Cooling *not* microprocessors

The latest  $\mu$ Ps have given rise to some ingenious new ways to keep systems from losing their cool. So far, though, veteran designers are waiting for proof of cost-effectiveness before warming up to these new technologies.

**Dan Strassberg, Senior Technical Editor**

Uh oh! Are those droplets of water *boiling* on top of your ICs? Nearly every engineer who designs a high-performance system using one of the hot new 32-bit  $\mu$ Ps must deal with the fact that the CPU, its SRAM cache, and the video controller can get really *hot*. To make the point, suppliers of cooling devices like to perform the boiling-water demo. Alas, as you'll see, that demo isn't so far-fetched. But beware—when a complex IC's case is at 100°C, the chip within it is well above the temperature at which its performance ceases to meet specs and where the IC's long-term reliability is likely to suffer.

The initial versions of Intel's Pentium dissipate as much as 16W. Digital Equipment Corp's 21064-AA Alpha AXP RISC  $\mu$ P, when operated at its maximum clock speed of 166 MHz, dissipates 23W. Although the pc boards on which you mount the ICs carry away significant heat, you have to work hard to maintain the devices' junction temperatures at or below 85°C (as specified for the 21064-AA) or 90°C (as spec'd for the Pentium).

In small systems, the hard work has traditionally involved adding heat sinks

and fans. Now, though, there are other alternatives, including liquid cooling technologies suited to small systems and techniques for reducing a CPU's power dissipation without affecting its performance. (See **box**, "Dynamic power management— $\mu$ P cooling's future.")

## **Don't try this at home!**

With no heat sink and with only free-air convection to cool it, the Pentium's junction-to-air thermal resistance is 11.7°C/W. If you try operating the device at its maximum clock rate in a 25°C (room-temperature) ambient without employing some cooling measures, the junction temperature will head for 212°C. The case temperature will head for about 200 °C—100°C *above* the temperature of boiling water and hot enough to melt solder. Before these conditions exist, the chip will fail. Only if you run the chip at a clock rate below one-third of its specified 66-MHz max can it operate indefinitely without cooling. Even then, you have to make sure that the ambient temperature doesn't exceed 25°C. If the ambient can reach 45°C, you have to limit the clock rate to 16 MHz.

High clock speeds and circuit com-



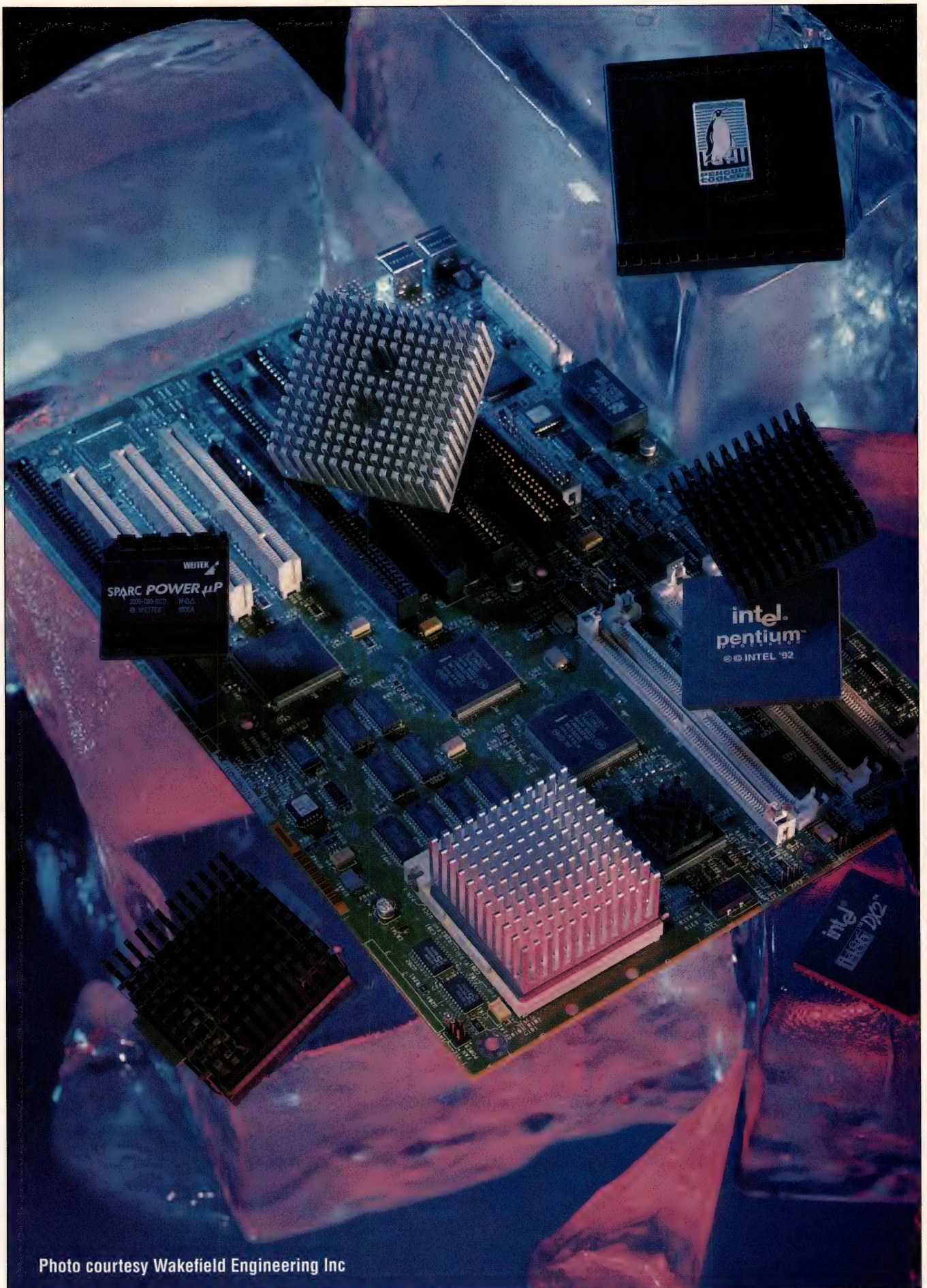


Photo courtesy Wakefield Engineering Inc



# Cooling *hot* microprocessors

plexity underlie the high temperatures. In a CMOS IC, if the feature size and supply voltage remain constant, the current drain (and hence the power dissipation) will be almost directly proportional to clock speed and gate count. So, unless there are changes in the IC-fabrication process, a new  $\mu$ P that has twice as many gates as its predecessor and runs at twice the clock speed consumes four times as much power.

The latest  $\mu$ P chips' high power dissipation has compelled many digital hardware designers to become familiar with a discipline they never had to worry about before—thermal management. Mostly, thermal management has been the province of mechanical engineers and of electrical engineers who design high-power equipment, much of which is analog in nature. Many digital designers who have only recently been forced to become responsible for thermal design appear to underestimate the field's complexity or at least its subtleties.

According to Dan Busby and Marty Pitasi of Hewlett-Packard's personal workstation operation in Chelmsford, MA, one of the worst mistakes you can make is to delay considering thermal issues until a product is in the final design stages. Worse yet is failing to think about thermal matters until the product is in production. The only correct time to start planning how to keep a product cool is at the beginning of the design cycle, the HP engineers assert.

Poorly conceived remedies for thermal problems abound, and some cures can be worse than the disease. Costly thermal-management measures have been known to yield products whose reliability is worse than that of similar products built before the measures were adopted. Such experiences can tempt you to ignore thermal design. Often, doing so will seem to work. If IC junction temperatures exceed operating limits by no more than, say, 10°C, the effects can be subtle—for example, increases in

setup and hold times and propagation delays. Such problems can fail to show up in routine production testing but then become obvious once the product is in customers' hands. At that point, finding a solution can damage your company's reputation and can cost far more than thermal-management approaches implemented during design.

## Keeping cool causes cost crunch

Cost plays a major role in thermal management. Both HP and DEC have so far shunned alternatives to forced-air cooling in their personal workstations; the companies are not convinced that other approaches can be as trou-

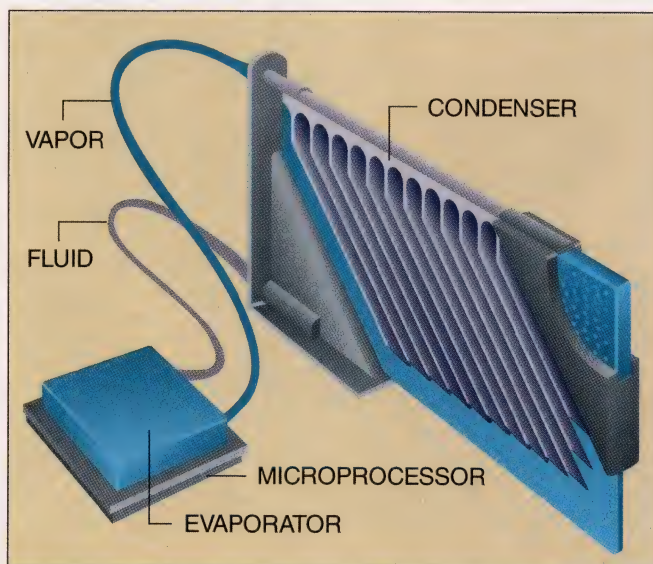
ble. Consequently, the vendors maintain, equipment that uses these techniques is more reliable than equipment that uses fans, and it does not make noise that can disturb a quiet office.

Aavid Engineering's recently announced Oasis technology is an example of a passive-cooling scheme that uses fluids. Strictly speaking, Oasis doesn't cool a piece of equipment; it transfers heat from one place to another. But if a product resides in an enclosure whose large outer surface is "washed" by cool, freely moving air, and you use the technique to move heat to one of the enclosure's outer walls from a hot  $\mu$ P buried deep inside, the distinction seems academic.

Oasis (**Fig 1**) works by having the hot component boil Fluorinert, a chemically inactive fluid. The boiling takes place in an evaporator—a network of tubes in contact with the hot device. The liquid boils at 57°C. Flexible plastic tubing carries the Fluorinert vapor to a condenser in a cooler area of the system and carries the condensed vapor (fluid) back to the hot component. The hot component never becomes warmer than 57°C as long as the air passing over the condenser removes enough heat to return the Fluorinert to its liquid state. As the Fluorinert vapor travels from the hot component to the condenser, it does give up some of its heat, warming the air

within the enclosure somewhat, but this should not be a major problem.

Another cooling scheme that uses Fluorinert is 3M Co's Liquid Heat Sink (LHS) (**Fig 2**). Among products that use technology of this type are portable Pentium PCs made by Dolch Corp (Milpitas, CA). LHS uses flexible plastic bags filled with Fluorinert to carry heat away from hot components. A common configuration sandwiches a bag between a pc board and a system enclosure's outer wall. Dimensional tolerances are a bit more critical than in air-cooled products; good heat transfer depends on maintaining the proper force on the bag, even though the fluid



**Fig 1—One of the newest and most intriguing cooling technologies is Aavid Engineering's Oasis. The hot component boils Fluorinert at 57°C. The vapor travels through tubes to a condenser where it again becomes a liquid and returns to the hot component. As long as enough heat is removed from the condenser, the component temperature does not exceed 57°C. (Drawing courtesy of Aavid Engineering Inc)**

ble-free or as cost-effective in relatively high-volume manufacturing. However, cooling approaches are very much a function of the application. HP's automatic test systems for high-speed digital ICs use liquid cooling. The IC test systems are many times larger and more costly than personal workstations and are produced in smaller quantities.

Nevertheless, proponents of some liquid-cooling approaches point out that their technologies not only compete in cost with air cooling but offer additional advantages. For example, several heat-transfer schemes that use liquids are both passive and silent. That is, they do not require motors or pumps to move



expands as it warms. Except for the loss of cooling, a leak can do no damage, however. Fluorinert doesn't conduct electricity or harm the earth's ozone layer. You can obtain LHS in a wide range of sizes. A 2.5×2.5×0.065-in. unit costs \$6.06 (5000).

Fluorinert figures in yet another cooling scheme: Heat Transfer Devices' (HTD's) heat sinks look ordinary enough from the outside but are filled with Fluorinert. The company claims that its devices exhibit a thermal resistance one-third that of solid aluminum heat sinks of similar dimensions. The HTD heat sinks are not cheap, though. Prices begin at around \$10 in large

quantities, a cost several times that of aluminum heat sinks of equal size.

**Table 1** is a list of cooling approaches. Of these, numbers 10 through 12 are unsuited to small systems and, therefore, lie outside the scope of this article. Numbers 1, 2, 7, 8, and 13 suit battery-powered portable systems as well as stationary equipment. The remaining techniques are appropriate for small and medium-sized stationary systems and for ac-powered portable equipment. The techniques that suit battery-powered equipment are or can be silent. So can the technique in number 6.

Fans and thermoelectric coolers (TECs) are not ideal choices for bat-

tery-powered equipment because these active cooling devices themselves consume power. Although fans and TECs can reduce the temperature of a system's hottest chips, they raise the product's total power dissipation and reduce the operating time between battery charges. Unlike fans, TECs do nothing to improve air circulation; their added dissipation usually increases forced-air cooling requirements. Indeed, applied without the requisite caution, TECs can actually raise the temperature of the chips they are supposed to cool! (See **Ref 1**.)

A popular way of cooling a single hot IC is with a fan/heat sink (**Fig 3**).

## Dynamic power management— $\mu$ P cooling's future

Dynamic power management technology (item 13 in **Table 1**) has to be the wave of the future in  $\mu$ P cooling. The idea is to make sure that a system's hottest chips dissipate no more power than they absolutely must to meet system performance requirements. Except in rare instances (instances that may occur only when a computer system is running a benchmark test suite), high-performance  $\mu$ Ps sit idle during a large percentage of CPU cycles. In other words, most of the time, a  $\mu$ P can perform just as well if its clock rate is lowered. Dynamic power management lowers the clock rate whenever doing so doesn't adversely affect performance.

Because a  $\mu$ P's power dissipation is almost directly proportional to clock speed, the technique can drastically cut dissipation and chip temperature. Dynamic power management is a more sophisticated version of the static power-management schemes used in modern notebook PCs. Static power management shuts down the display and slows the CPU clock if the user doesn't press a key or touch the mouse or the trackball for a predetermined interval. At other times, the display and the CPU dissipate full power.

All techniques that limit the dissipation of a system's hottest chips offer benefits beyond reduced cooling requirements: Limiting dissipation saves energy in accordance with the US Environmental Protection Agency's Energy Star program for computing equipment. In desktop PCs, lower standby-power requirements raise the possibility of combining a low-cost battery-backup system with the power supply. In battery-powered systems, reduced dissipation allows longer operation between charges. And, of course, lower operating temperatures improve system reliability.

PicoPower's Power On Demand (POD) and EliteGroup's PowerShift exemplify what dynamic power management is all about. Both techniques continuously monitor the CPU and dynamically adjust the clock to minimize the number of idle cycles. POD also algorithmically computes the CPU's junction temperature. When the  $\mu$ P runs at full clock speed long enough that the junction temperature would otherwise become excessive—a rare occurrence—POD slows the clock. Only at such times does performance degrade. PowerShift

does the same thing by sensing the  $\mu$ P's case temperature.

PicoPower demonstrates POD by continuously running the same performance-metric software on a pair of identical  $\mu$ Ps. POD controls one chip's clock while the other one's clock always runs at full speed. The performance scores of both chips remain identical, yet the package of the IC that runs at full speed soon becomes too hot to touch. The case of the unit running under POD control never becomes much warmer than that of an unpowered chip.

PicoPower is an IC vendor. The company has implemented POD in a pair of 2-chip sets, the Fir and Redwood system controllers for use in 486 PCs. Each set costs under \$30 in large OEM quantities. Samples of the Redwood are available now; samples of the Fir will be available this quarter.

EliteGroup does not sell ICs. The company is a major manufacturer of PC mother boards (annual sales of approximately \$240 million) with facilities in both the United States and Asia. EliteGroup offers PowerShift on its mother boards, including boards that contain Motorola PowerPC chips. The company also recently announced SoftShift, a software package for MS-DOS and Windows that implements power management in PCs that contain the company's mother boards. The package will be free to purchasers of those PCs. This year, the vendor expects to offer a \$29 version of the package that will work on PCs whose mother boards come from other manufacturers.

Adjusting the clock rate is a bit more complex than the preceding paragraphs suggest. With CPUs that contain dynamic registers, the minimum clock rate is fairly high. With  $\mu$ Ps that allow stopping the clock, interrupt latency can be a problem, especially in embedded applications. PicoPower's alliance with National Semiconductor has addressed this problem. National has developed several peripheral-controller chips that work with the PicoPower chip sets. When one of these peripheral controllers senses a condition that demands a quick response from the CPU, the peripheral controller sends a signal to the PicoPower system controller, which boosts the CPU's clock rate.



# Cooling

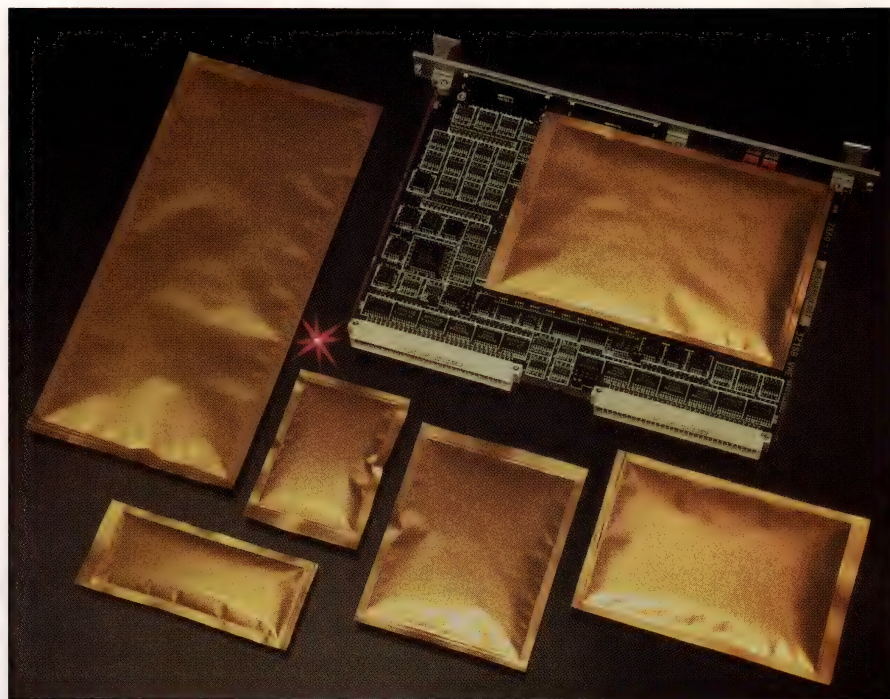
## hot

### microprocessors

These devices, which integrate heat sinks and subminiature brushless de-powered tubeaxial fans, are available from many sources, some of which are listed in the manufacturers **box**. Fan/heat sinks for use in PCs include a connector that mates with an unused connector on the PC's power supply. Fan/heat sinks cost about \$9 to \$14 in large OEM quantities and less than \$30 in small quantities. Those prices are slightly less than the cost of separate fans and heat sinks. Since effort is involved in making your own fan/heat sink from the separate parts, the combination is more economical.

Fan/heat sinks offer a practical way to cool hot  $\mu$ Ps in some situations, such as when you upgrade a design to use a higher performance  $\mu$ P that runs hotter than the one it replaces. You should recognize fan/heat sinks' limitations, though. One is temperature. Most units are recommended for operation at temperatures of 60°C or less. Under these conditions, you can expect roughly 10% of units to fail in 10,000 hours (approximately 14 months) of continuous operation. Higher temperatures reduce the bearing life.

If you use a fan/heat sink with a Pentium  $\mu$ P that dissipates 16W in air whose maximum temperature is a relatively cool 32°C, the fan must move air past the heat sink at a speed of at least 200 linear ft/minute (LFM) to maintain the IC's junction temperature at 90°C or less. (With air moving past the heat sink at this speed, the IC's junction-to-air thermal resistance drops to



**Fig 2—Not all heat sinks are solid. 3M Co's Liquid Heat Sink uses flexible plastic bags filled with Fluorinert liquid to carry heat away from hot components.**

3.6°C/W.) The most popular fan size in fan/heat sinks is 40 mm in diameter. Most such fans can move air at 200 LFM if their air-exit path is not severely impeded. (Generally, in fan/heat sinks, air enters through the heat sink and exits through the fan.)

If the IC's junction temperature is 90°C, its case temperature will be 80°C. Since the fan makes thermal contact with the IC case by way of the heat sink attached to it, the fan's temperature will be close to 80°C. At that temperature, the fan's life expectancy may be too short to satisfy you. The fan runs cooler and more reliably if it is separate

from the heat sink and mounted a short distance from the  $\mu$ P. Simple duct work might allow it to deliver the full airflow to the heat sink. Few systems allow room for this approach, however.

This scenario underscores the importance of having a backup in case the fan in the fan/heat sink fails. If the fan stops moving air, the fan/heat sink may actually impede airflow. Therefore, you should consider a scheme that senses the IC's case temperature or the fan's airflow and slows the  $\mu$ P clock if the fan ceases to operate.

Note that you can't easily use a fan/heat sink with DEC's 21064-AA  $\mu$ P, although you can use a separate fan. Each of the IC's three package options includes an integral heat sink and mounting studs that aren't well suited to direct attachment of a fan. Unlike other  $\mu$ P packages, the metal parts (including the studs) are in electrical contact with the back of the die. This approach, which minimizes the junction-to-case thermal resistance, should cause no unusual electrical problems; the back of the die is at ground potential.

An area that seems trivial but isn't is how to attach a heat sink (or a fan/heat sink) to a  $\mu$ P or other high-pin-count IC. Heat-sink attachment can definitely cause problems for the unsuspecting. Today, almost all high-pin-count chips

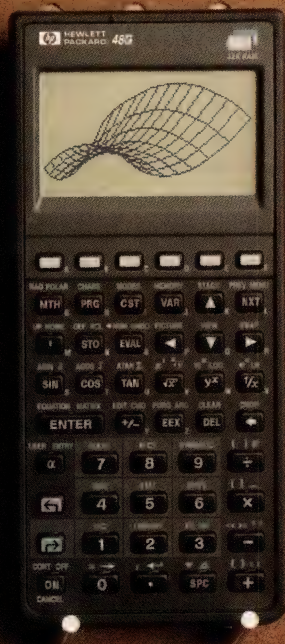
## Looking ahead

In the near and intermediate term, two factors will slow  $\mu$ Ps' rush toward meltdown. These factors are reduced supply voltages and the techniques described in the **box**, "Dynamic power management— $\mu$ P cooling's future." In the short run, then, the industry is likely to see chips that are just as capable as existing ones but that run significantly cooler.

Ultimately, though, chip designers will see power-reduction technologies as the key to producing even faster  $\mu$ Ps and support chips that dissipate no more power than today's fastest devices. So the cooling technologies described here will remain important. Surely, liquid and biphasic (liquid/gas) cooling techniques such as Aavid's Oasis technology will grow in importance over time. The fact that biphasic cooling is passive and silent makes it very attractive. Whether vendors can turn skeptics into converts will depend on their ability to show that the techniques are cost-effective in products manufactured in significant quantities.





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## Cooling *hot* microprocessors

are in pin-grid-array (PGA) or surface-mount packages—thin quad flatpacks (TQFPs), for example. You can solder a PGA into through holes or place it in a conventional- or a zero-insertion-force (ZIF) socket. On rare occasions, a PGA is surface-mounted by using a solder-reflow process to attach it to a pattern of lands on a pc board. Chips mounted with any of these attachment methods except the last one can tolerate large forces parallel to the board. Surface-mount packages that are soldered in

place are not so tolerant, however. Repeated application and removal of forces parallel to the board can actually crack the solder joints that hold these packages on the board.

Most heat sinks are made of aluminum, which has a thermal coefficient of expansion (TCE) different from that of IC packages. If you use a rigid thermally conductive cement or epoxy to attach a heat sink to a TQFP, the leads are subjected to changing forces in the plane of the board each time the IC heats or cools. Except for this problem, the cement is a good choice. The tops of IC packages aren't perfectly flat. The

cement fills gaps between the heat sink and the package that can materially reduce the heat sink's effectiveness.

In fact, Intel reports that attaching a heat sink to a Pentium chip without interposing a thermally conductive material to improve the contact can more than double the IC's junction-to-heat-sink thermal resistance (Ref 2). An increase this large can cause serious problems. Alternatives, such as thermally conductive double-sided adhesive tape and adhesives that never completely solidify, are popular in some quarters. However, several companies report that such materials can lose their stickiness over time and that few

## Manufacturers of $\mu$ P-cooling products

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Note: Many of the listed companies supply cooling products in categories other than the one(s) shown after the company name. Also note that some products (fan/heat sinks, for example) fit into more than one category.

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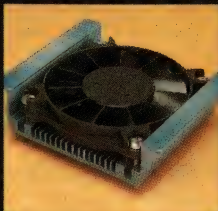
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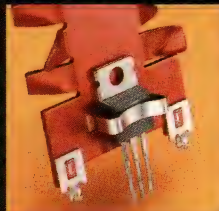
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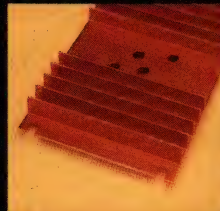
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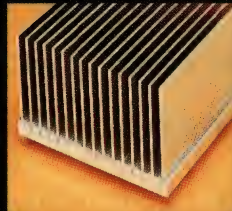
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# Cooling *hot* microprocessors

adhesive tapes offer thermal resistance as low as that of good quality thermally conductive epoxy.

For those who would like to use epoxy to attach heat sinks to their surface-mounted ICs but who are concerned about the differential-TCE problem, Wakefield Engineering offers a solution in its proprietary Deltem heat-sink material. Deltem's TCE matches that of IC packages; its thermal conductivity is nearly as good as that of aluminum, and its price is even lower. According to the vendor, Deltem heat sinks often cost only half as much as aluminum ones.

The company's competitors insist that you can solve the differential-TCE problem simply by not using a rigid adhesive. Instead, they suggest mechanical attachment means. For example, if you make the heat sink a bit larger than the IC, you can bolt the heat sink to the PC board on which the IC is mounted. Or you can use spring clips

that engage slots in the board. Spring clips are a favorite means of attaching heat sinks to socketed ICs as well as to PGAs. Unlike TQFPs, PGAs do not have leads along their outer edges that

interfere with clips. Some sockets contain recesses especially designed to engage heat-sink attachment clips.

When you attach a heat sink with bolts or clips, another contro-

**Table 1—Some ways to cool electronic equipment**

1. Natural convection in air
2. Natural convection in air with heat sink(s)
3. Forced-air cooling of the equipment enclosure; no heat sinks
4. Forced-air cooling of the enclosure; heat sinks on hottest devices
5. Same as 4, except using a liquid-filled heat sink (HTD Inc)
6. Same as 4, except with active heat sink(s) (fan/heat sinks) or impingement cooling
7. Same as 1 or 3 with 3M Liquid Heat Sink (Fluorinert-filled bag)
8. Same as 1 with the addition of heat pipes or Aavid Engineering's Oasis biphase technology (vaporizing/condensing Fluorinert)
9. Add thermoelectric coolers to 1, 2, 3, 4, or 6
10. Immersion of pc boards into recirculating Fluorinert, which, in turn is cooled by mechanical refrigeration
11. Transfer of heat from hottest components to cold plates, which, in turn transfer heat to surfaces whose temperature is maintained by a refrigerated liquid
12. Same as 3 or 4, but with mechanical refrigeration or an air-to-liquid heat exchanger to cool the air that circulates within the enclosure
13. Any of 1 through 12 in combination with EliteGroup's PowerShift or PicoPower's Power On Demand (POD) dynamic power-management technology.

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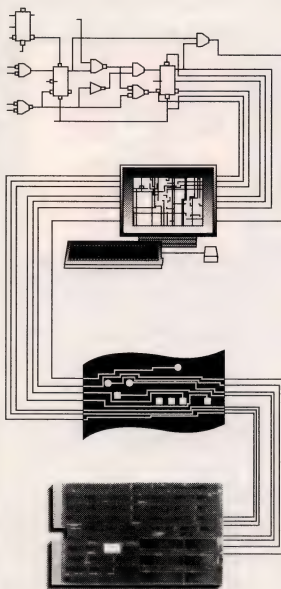
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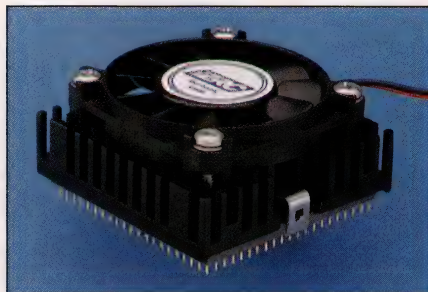


## Cooling

## hot

versial subject is whether to use a thermally conductive washer or a thermally conductive nonadhesive paste (heat-sink compound or thermal grease) between the IC package and the heat sink. Several companies listed in the manufacturers box provide such materials. Although these materials can reduce the thermal resistance between IC packages and heat sinks enough to spell the difference between a cooling scheme's success or failure, some companies balk at the logistical problems created by using the materials. For example, companies wonder whether service people who replace ICs in the field will remember to reapply heat-sink compound or install new washers. Others recall older heat-sink compounds that are no longer sold. After prolonged exposure to high temperatures, these materials could change from thermal conductors to insulators!

A material from which you can make your own washers is Ucar Carbon Co's



**Fig 3—Fan/heat sinks, such as this one from IERC, offer a practical way to cool hot  $\mu$ Ps—for example, when you upgrade a design to use a higher performance  $\mu$ P that runs hotter than the one it replaces. These devices are not a panacea, however. (Note the clip used to attach the fan/heat sink to a PGA.)**

Grafoil. (The name is a contraction of "graphite foil.") Grafoil is pure carbon; hence, it is electrically as well as thermally conductive. The electrical conductivity prevents its use in washers for power transistors; their cases are often at high voltages. It poses no problem in IC washers, however. For a little over \$30, you can buy a roll of 0.015-in.-thick Grafoil large enough to make 900 2x2-

in. washers. The material's heat-transfer properties have earned a good reputation among engineers who package electronic systems. Though it makes no endorsements, **Ref 2** suggests that you'll be hard-pressed to find anything better. Unfortunately, though, detailed thermal data are not available. **EDN**

## References

1. Lancaster, Don, Thermoelectric review in the "Hardware Hacker" column, *Electronics Now*, October, 1993, pg 71.

2. Intel Corp application note AP-480 (order no. 241575-001), *Pentium processor thermal-design guidelines*, April, 1993. (Intel is preparing a new, expanded version that may be available by the time you read this.)

*Sr Technical Editor Dan Strassberg can be reached at (617) 558-4205; fax (617) 558-4470; E-mail EDNStrassberg@MCI-MAIL.COM; EDN BBS: EDNStras.*

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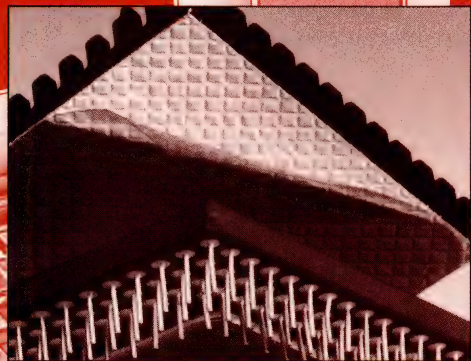
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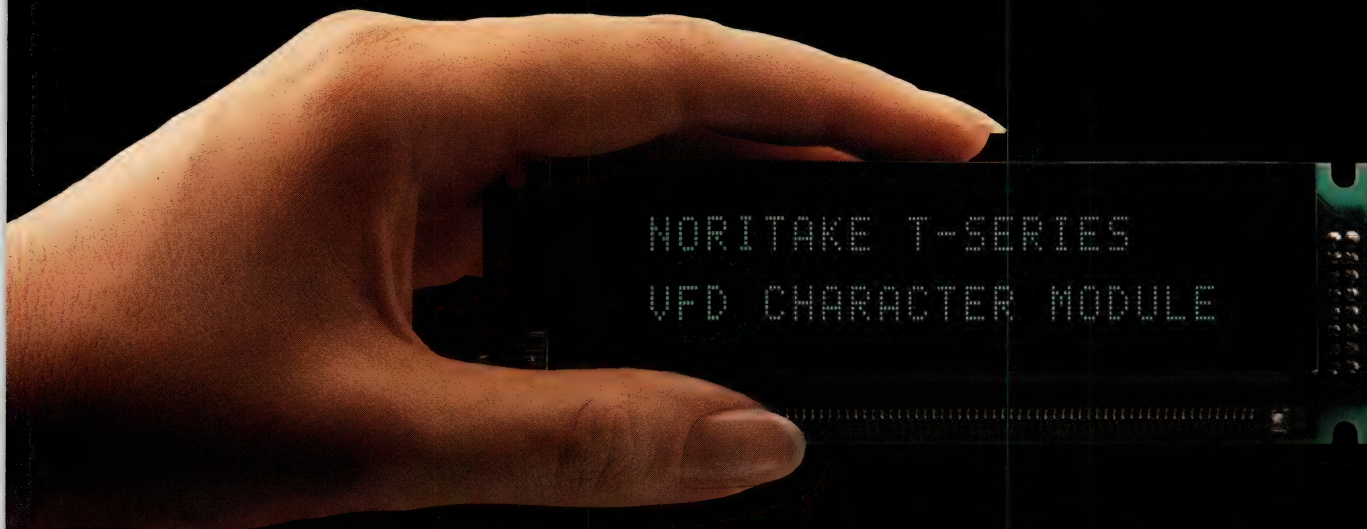
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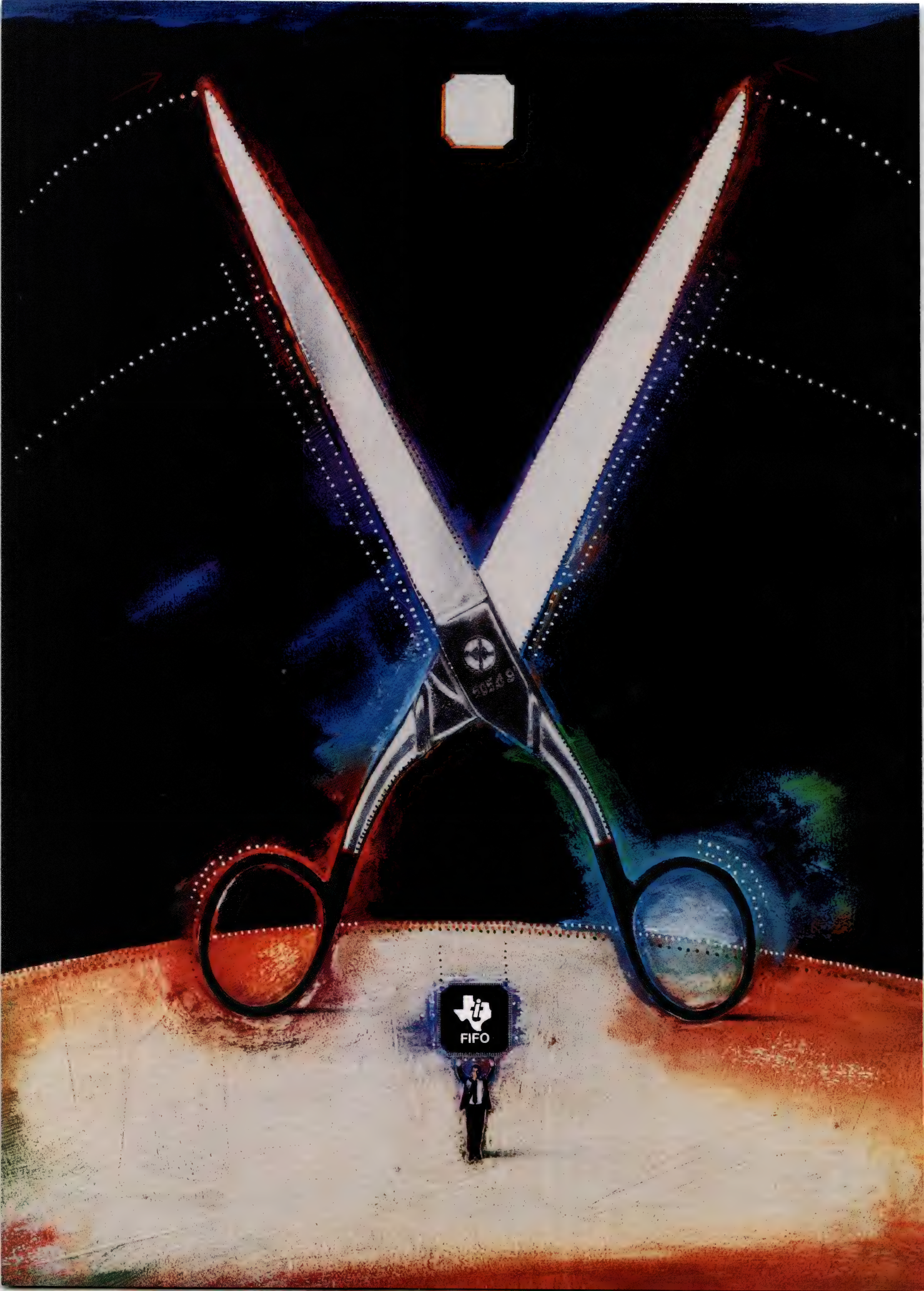
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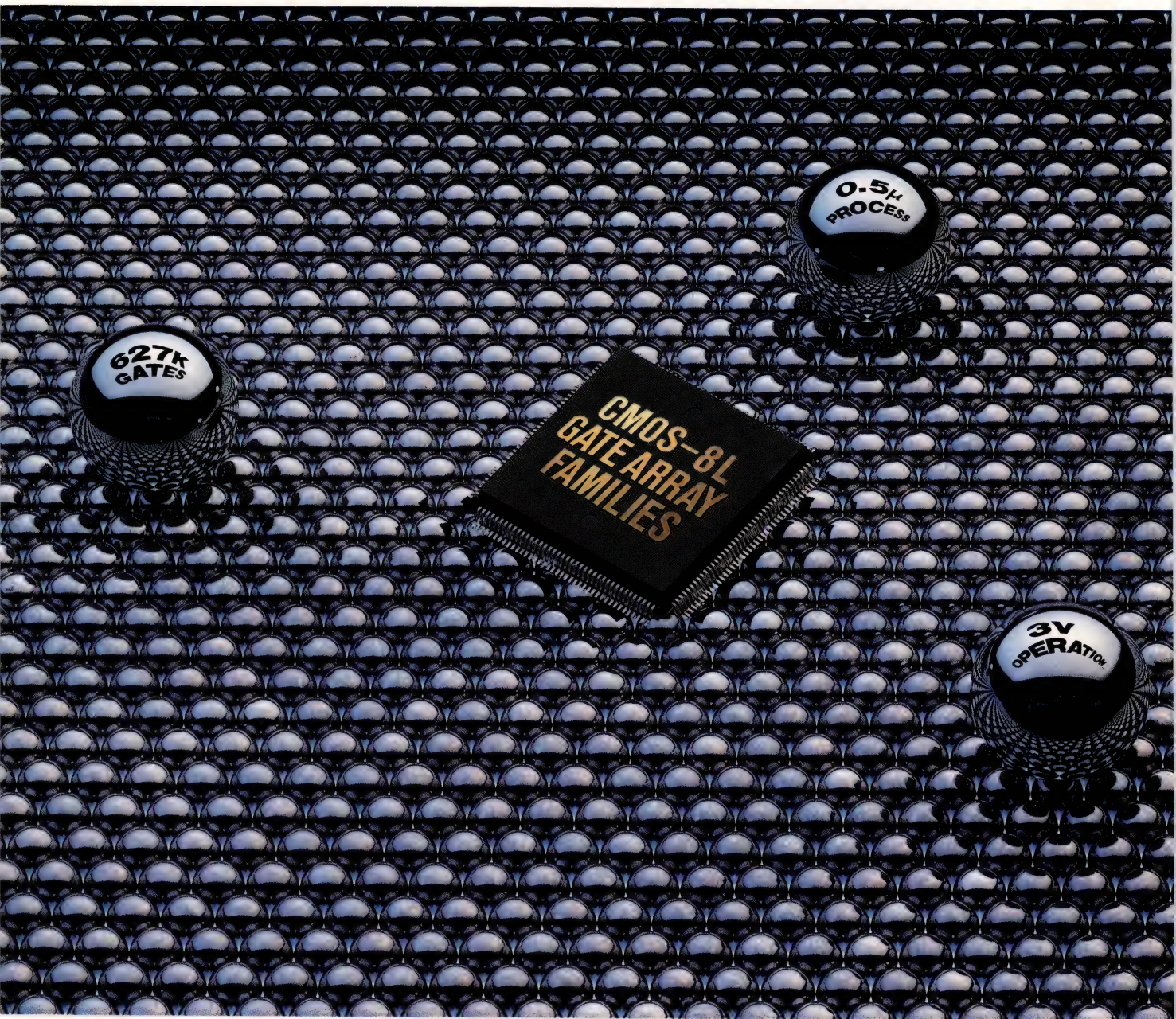
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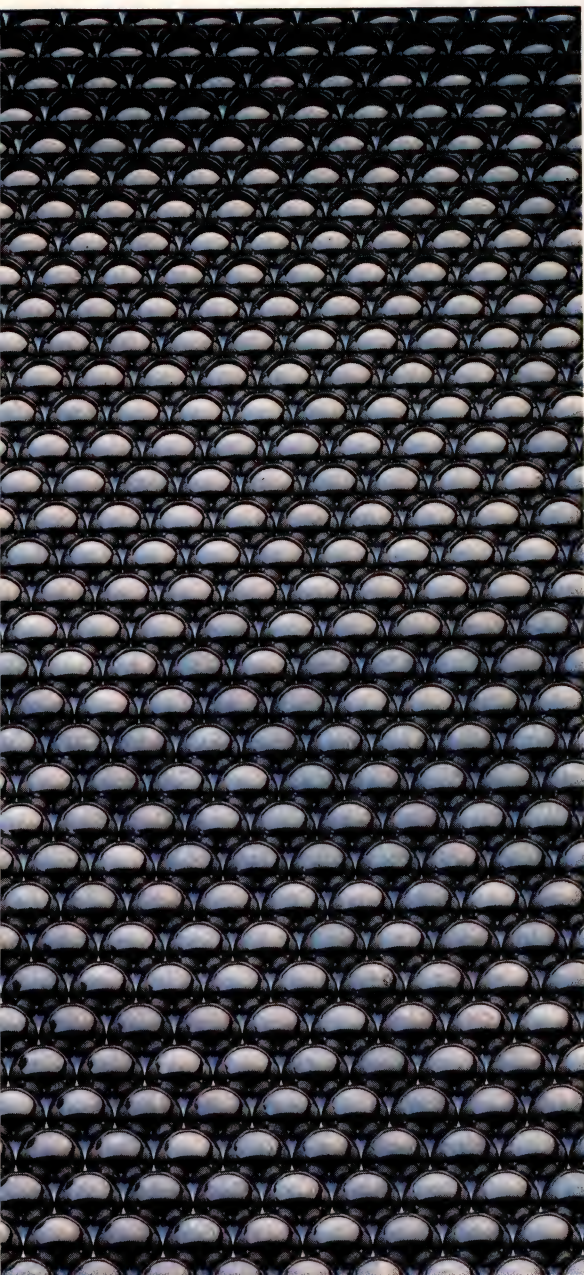
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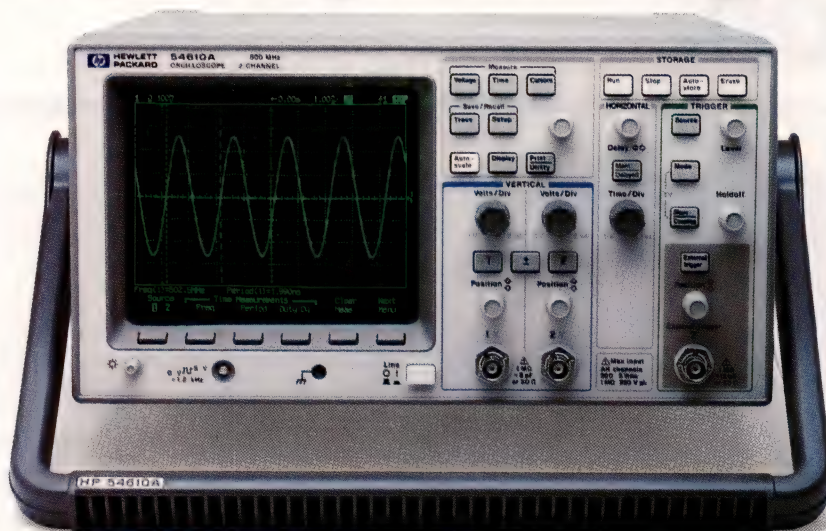
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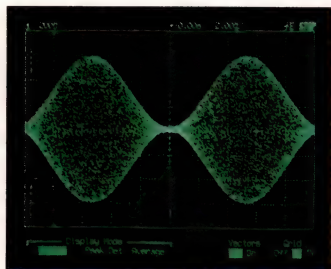


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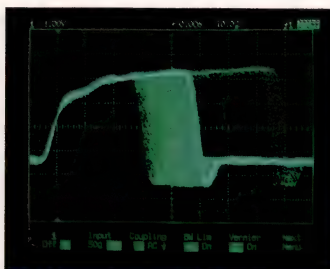


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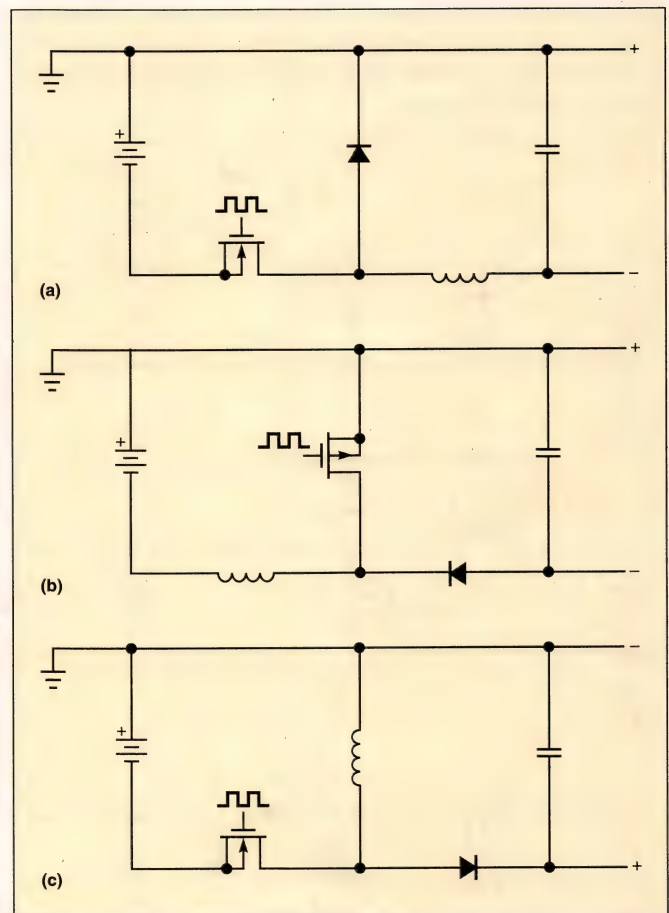
Bruce D Moore, Maxim Integrated Products

*Power supplies are perhaps the most crucial elements of a battery-powered system. Knowledge of some basic regulator topologies will help you select or design the right supply configurations for your needs.*

Portable computers and digital assistants usually require more than one power supply. These devices may need an ac/dc adapter or battery charger; a high-voltage dc/ac converter for the backlight; and other supplies for lasers, cellular radio transmitters, and auxiliaries. Swapping components in a basic switching-regulator layout alters the circuit topology to create regulators that step up, step down, or invert an input voltage. Substituting a transformer for the inductor produces at least two more regulator circuits or auxiliary output voltages.

The parameters affecting the choice of a switching-regulator topology include the peak currents for the load and inductor, the voltage level on the power transistors, and the necessity for magnetic and capacitive energy storage. **Table 1** shows the seven most common regulator topologies beginning with the simplest (top of **table**) (which are generally also the most desirable in terms of efficiency, cost, and size) and progressing to more specialized types (bottom). The **table** also lists the pros and cons of each topology, allowing you to scroll through and find the topology that meets your needs.

The **table** omits complex topologies such as resonant-mode regulators because their control circuitry consumes too much power for small battery-operated systems. The simpler the circuit, the better: Simple circuits have no magnetics at all or have simple inductors or 1:1 transformers. Off-the-shelf magnetics simplify assembly and minimize costs. Textbooks and magazine articles list other topologies that you can derive from the basic topologies in **Table 1**. Examples include the Cuk converter, which combines the buck and boost topologies, and the forward converter, which combines a



**Fig 1—You can invert the input source to create three topologies. The negative buck regulator (a) has an output voltage less than the input. The negative boost regulator (b) has an output more negative than the input. The negative-inverter regulator (c) converts a negative voltage to a positive voltage.**

buck converter with half of a push-pull converter.

Switch-mode regulators have two fundamental modes of



## REGULATOR TOPOLOGIES

operation: discontinuous conduction and continuous conduction. Discontinuous conduction lets the inductor current decay to zero during each off period, which causes a transfer of all the stored energy to the output filter during each switching cycle. In the continuous-conduction mode, the inductor current includes a dc component proportional to the load. Operating in the continuous-conduction mode lowers the ratio of peak inductor current to dc-load current, thereby lowering the peak-to-peak ripple current and reducing the core loss.

### Peak current is critical

In battery-powered converters, the peak inductor current is important because it affects the battery life and parasitic losses. The peak currents depend partly on the average load current, which varies with the regulator topology. **Ref 1** presents equations for the peak-vs-load current associated with three regulator topologies. Peak inductor current also depends on the control circuit and whether the inductor current is continuous. The voltage stress on the switching transistor is usually not an issue in battery-powered converters. The 20 and 50V breakdown voltage ratings for standard logic-level MOSFETs are adequate for the low input and output voltages found in battery-powered systems.

Dissipation losses occur in the parasitic resistive elements of the regulator circuit. These losses include: the series resistance of the battery; the equivalent series resistance (ESR) of the filter capacitors; the on-resistance of the switching element; and the resistances in the conductors, connectors, and wiring. Dissipation losses are proportional to the square of the peak current, so reducing the peak current can greatly minimize these losses. In addition, internal heating degrades a battery's chemistry, so excessive peak currents can shorten a battery's life.

The best choice for most battery-powered applications is the buck regulator, provided you can afford the several cells needed to generate a battery voltage higher than the output voltage. Inductor current flows to the load during both phases of the switching cycle, so the average output current equals the average inductor current. In theory, the best efficiency occurs when the input voltage is low, which implies fewer battery cells in series. Assuming the switch's on-state voltage drop is much smaller than the input voltage, a low input voltage reduces the ac switching losses and the rms input current.

The boost, or step-up, topologies generate an output voltage that is greater than the input voltage. The boost topologies suit systems with a limited number of battery cells. Because the source voltage and the inductor are in series, the average inductor current equals the dc input current given by:

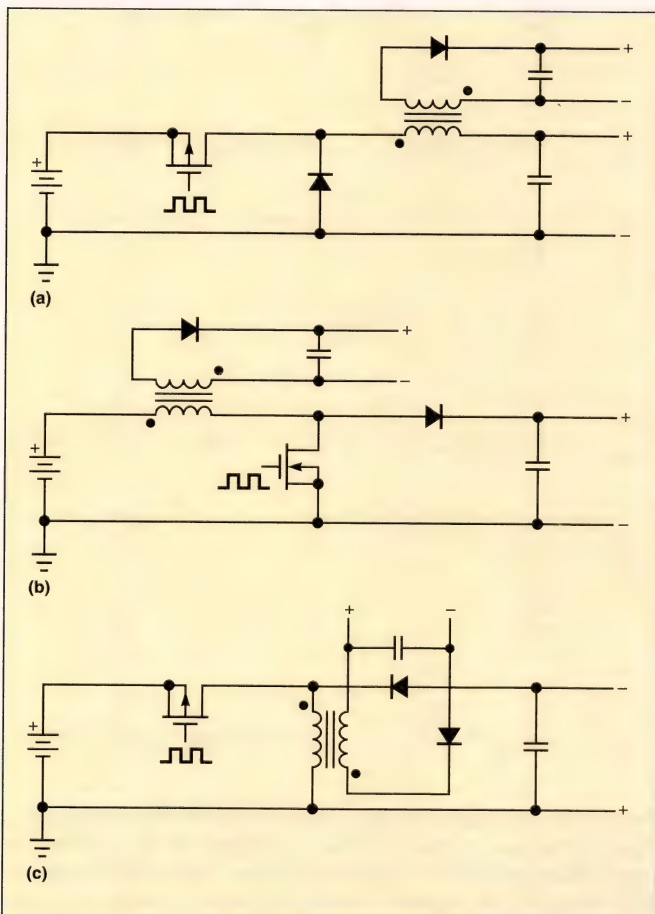
$$I = P_{in} / V_{in}$$

Sometimes called the buck-boost circuit, the inverter topology generates an output voltage that has opposite polarity from the input voltage. Inverting and flyback regulators are electrically equivalent when considering peak currents and voltage stress. These topologies are most suitable to applications that require negative or galvanically isolated outputs. In general, however, the high peak currents make inverting and flyback topologies the least attractive of the simple regulators.

Inverting and boost topologies operate similarly; however, the inverter's rectified inductor current produces a negative output voltage, which is not aided by the source voltage. The inverting regulator's switching element experiences large voltage swings that impose high switching losses and high stress on the switching transistor. In addition, both the input and output filter capacitors for an inverting or flyback regulator must absorb current waveforms that have large, sharp transitions. Fast-moving waveform edges are absent at the input capacitor of a boost regulator or the output capacitor of a buck regulator.

### Upside-down topologies have low-side switch

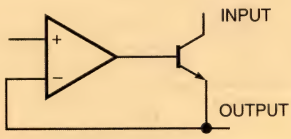
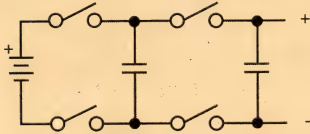
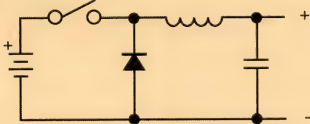
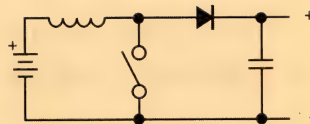
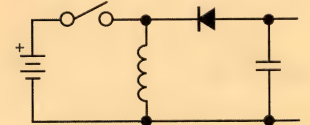
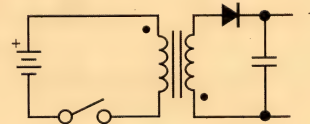
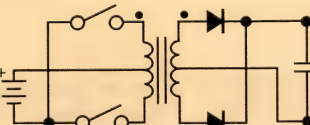
You can implement three negative topologies by connecting the classic buck, boost, and inverting topologies upside down. Because the input source is inverted, you must reverse the polarities for the switch and rectifier (**Fig 1**). Although there are no ICs currently available for the negative topologies, you can use a positive-output IC. Negative buck regulators enjoy all the advantages of positive buck regulators and have the added benefit of a low-side switch. The low-side switch arrangement allows the use of a low  $R_{on}$  n-channel



**Fig 2—You can create auxiliary outputs by using a flyback transformer instead of an inductor in the basic buck (a), boost (b), and inverter (c) configurations.**

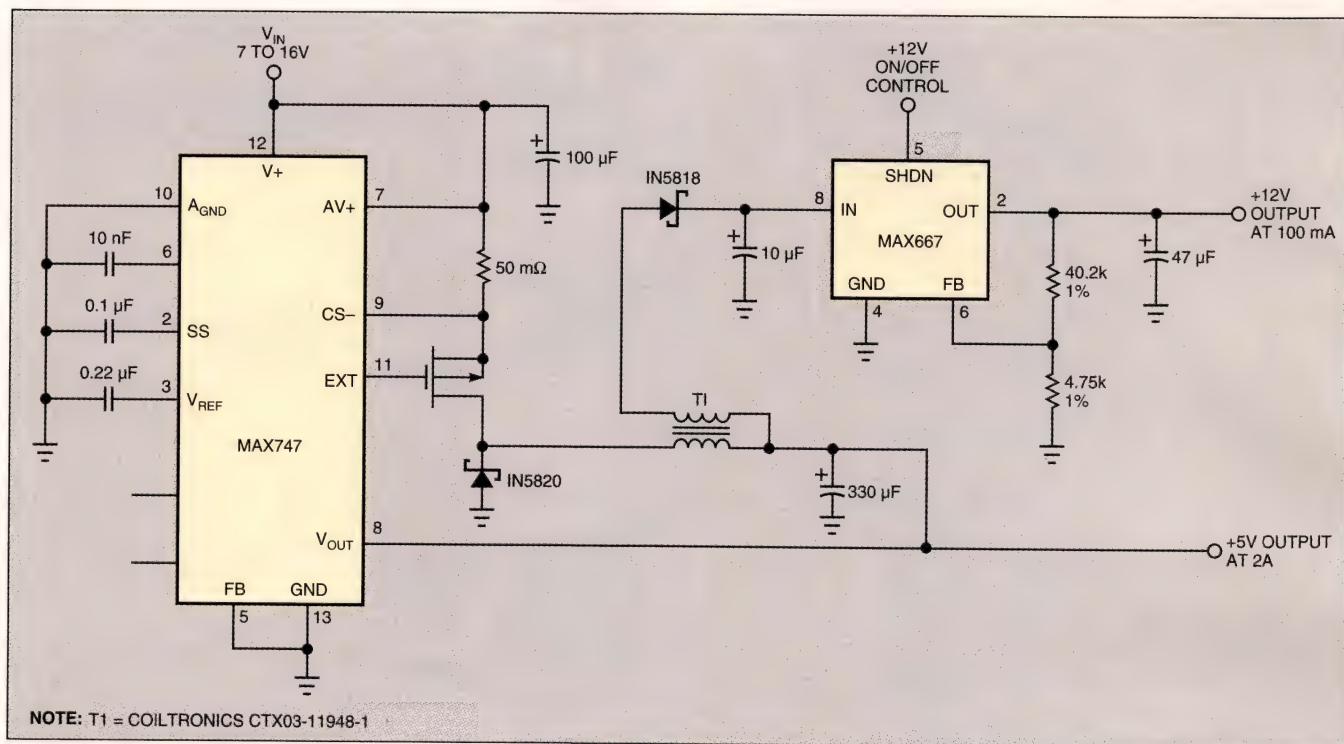


## Table 1—DC/DC topology hierarchy

	Pros	Cons
	<b>Linear regulator</b> Inexpensive Very small Low quiescent current Low noise/EMI	Only steps down ( $V_{out} < V_{in}$ ) Inefficient at high input voltages
	<b>Charge pump</b> Inexpensive Very small Can boost or invert	Limited output power Limited range of input/output voltage ratio
	<b>Buck</b> Lowest peak current Only one switch voltage drop Low-ripple current in output-filter capacitor Simple inductor Low switch-stress voltage	Only steps down ( $V_{out} < V_{in}$ ) High-side switch
	<b>Boost</b> Low peak current Low-side switch Simple inductor Low switch-stress voltage	Only steps up ( $V_{out} > V_{in}$ ) Output can't be completely turned off No short-circuit protection
	<b>Inverter</b> Simple inductor	Negative output only High-side switch High peak currents
	<b>Flyback</b> Isolated output Multiple outputs Steps up/down, inverts Low-side switch	Transformer instead of inductor High peak currents High switch-stress voltage
	<b>Push-pull</b> Isolated output Multiple outputs Steps up/down, inverts Core doesn't need to store energy Easy to filter	Complex transformer Two switches required Two rectifiers required



## REGULATOR TOPOLOGIES



**Fig 3—The buck regulator with coupled inductive flyback winding is the best choice for battery-powered systems. The configuration has low peak currents and low ripple in the output voltage.**

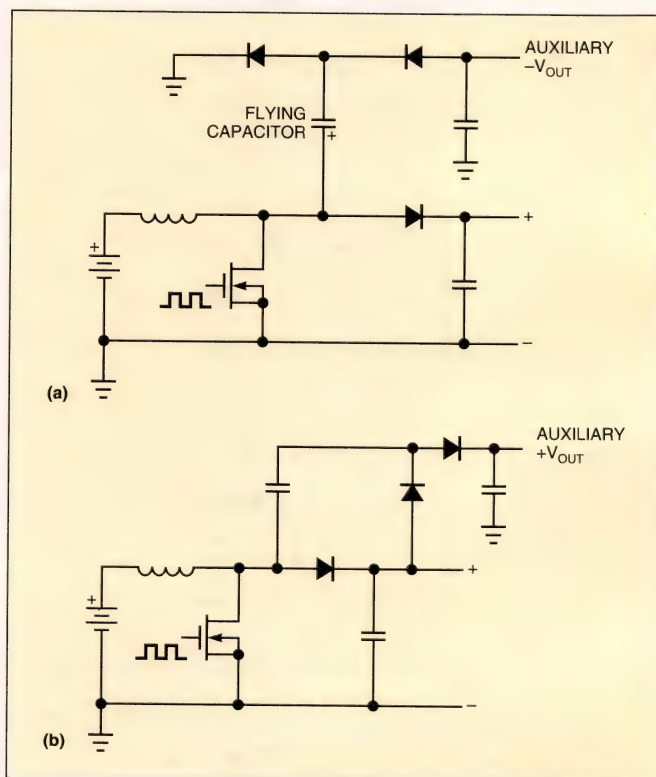
MOSFET with simple drive requirements. The negative buck regulator has some appeal as an alternative for the main positive regulator, provided the battery can float with respect to system ground. If battery floating is possible, you can refer ground to the negative output and the battery's positive terminal to  $V_{\text{out}}$ .

Usually, the best way to design multiple outputs in a battery-powered system is to build several independent supplies. Using simple topologies, you can generate the remaining outputs using off-the-shelf transformers or charge-pump taps.

Coupled-inductor circuits (**Fig 2**) add an extra flyback winding to the basic buck, boost, and inverting topologies. These hybrid circuits are important because they combine the advantages of a flyback circuit (isolation and inexpensive multiple outputs) with the benefits of the buck and boost circuits (low peak current and low voltage stress on the switch). The coupled inductor circuit reduces by one the number of windings required by a flyback circuit. This reduction allows the use of an inexpensive 1:1 transformer to generate dual output voltages.

The buck regulator with a flyback winding is the superior-performance topology for many battery-powered applications (**Fig 3**). The configuration has excellent stability, low peak currents, and low output ripple. The output power from the secondary winding depends on the main output's load current and the amount of differential voltage across the primary. Both of these parameters determine the change in core flux that triggers the flyback mechanism.

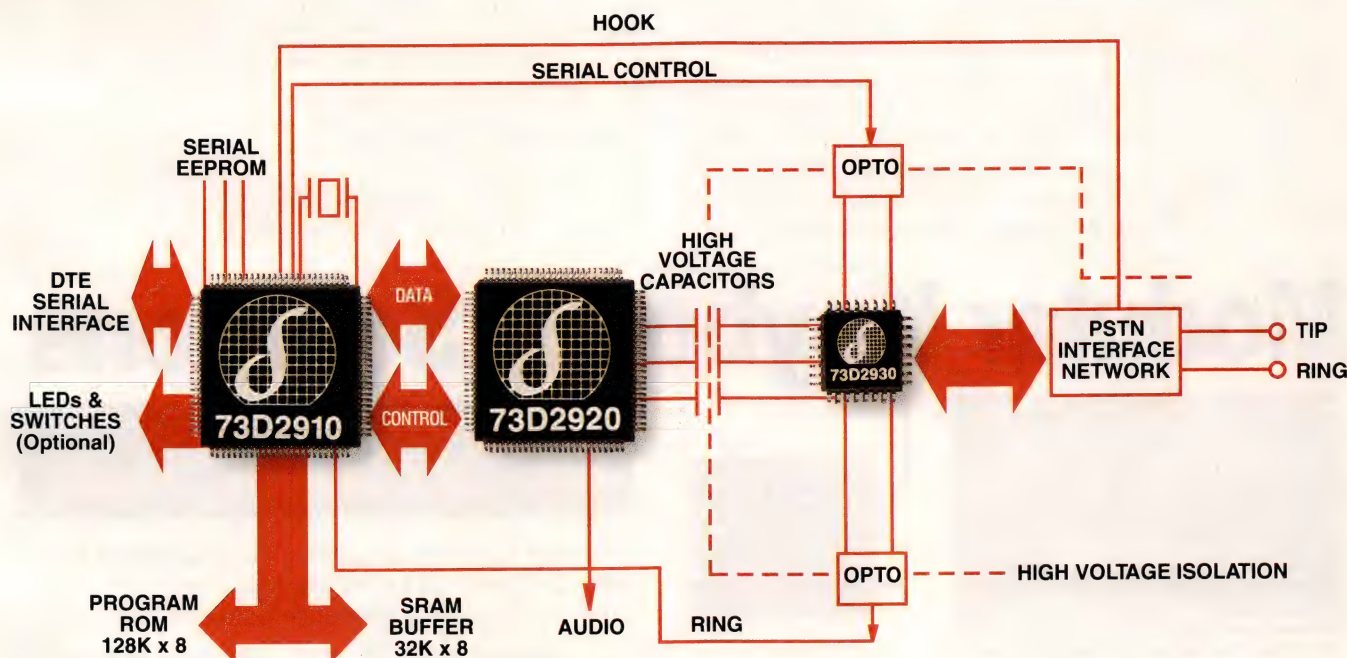
As a rule of thumb, the total secondary power available is equal to or less than one-half the main output power. This rule applies only to high input voltages. You should reduce the estimate of secondary power for input voltages less than one and



**Fig 4—The charge-pump tap offers an inexpensive way to achieve an auxiliary output voltage. Tapping a boost circuit with a flying capacitor (a) creates a negative charge pump. Placing a voltage doubler on the output of a boost circuit (b) creates a high-voltage auxiliary output.**



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## REGULATOR TOPOLOGIES

one-half times the output voltage. The rule also doesn't apply to circuits containing a synchronous rectifier instead of a simple diode. Synchronous rectifiers have a brief period when the primary current reverses, which causes the circuit to behave as a forward converter instead of a flyback converter. To transfer power efficiently during this forward conduction mode, you must minimize leakage inductances, reduce winding and rectifier impedances, and make the secondary output's filter capacitor as small as the ripple voltage allows.

Diode-capacitor charge pumps offer another inexpensive way to generate multiple output voltages. Any node having repetitive pulses can drive the diode-capacitor network. The gate-driver output or the main switching node of a switching regulator are good candidates. Boost regulators, for example, can charge a flying capacitor through a grounded diode when the switching node is high (Fig 4a). Turning on the boost transistor forces the switching node and the flying capacitor's positive voltage end to 0V. When the boost transistor turns on, the flying capacitor generates a negative voltage by discharging into the auxiliary output capacitor.

Diode-capacitor charge pumps work best with boost switching regulators because the switching node swings between a well-defined voltage  $V_{out}$  and ground. Therefore, the line regulation is good. The line regulation is not as good when you tap the switching node of a buck or inverting regulator because the high voltage  $V_{in}$  varies with battery volt-

age. Load regulation depends mostly on the diode's forward voltage drop. In very low-power applications (20 mA or less) where an output powers an op amp or an FET-gate driver, you can build the charge pump using an inexpensive 1N4148 diode and a 1- $\mu$ F capacitor.

EDN

## Reference

1. "Battery Management and DC-DC Converter Circuit Collection:," Appendix A, Maxim application note, 1993.

## Author's biography



Bruce D. Moore is a senior scientist with Maxim Integrated Products in Sunnyvale, CA. In his position, he plans new IC products for power-supply applications. In the three years he has been with his current employer, he has developed precision op amps, linear arrays, and power supplies for notebook and palmtop computers. Moore graduated with a BSEET from Heald Engineering College, San Francisco, CA, in 1977 and is currently taking classes at San Jose State University. Moore is also a member of the Golden Key Honor Society. His spare-time interests include motorcycle road racing, military history, and miniature bull terriers.

Article Interest Quotient (Circle One)

High 588 Medium 589 Low 590

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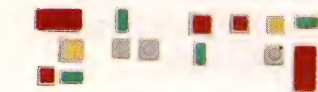
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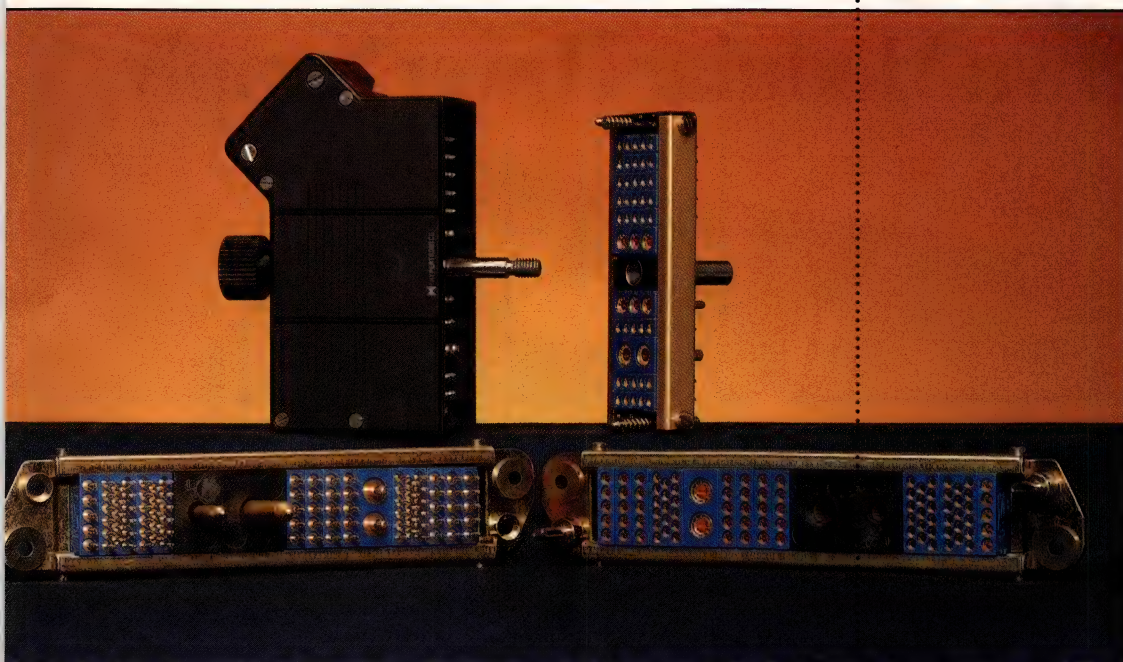
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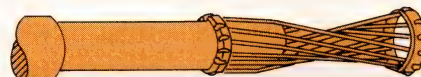
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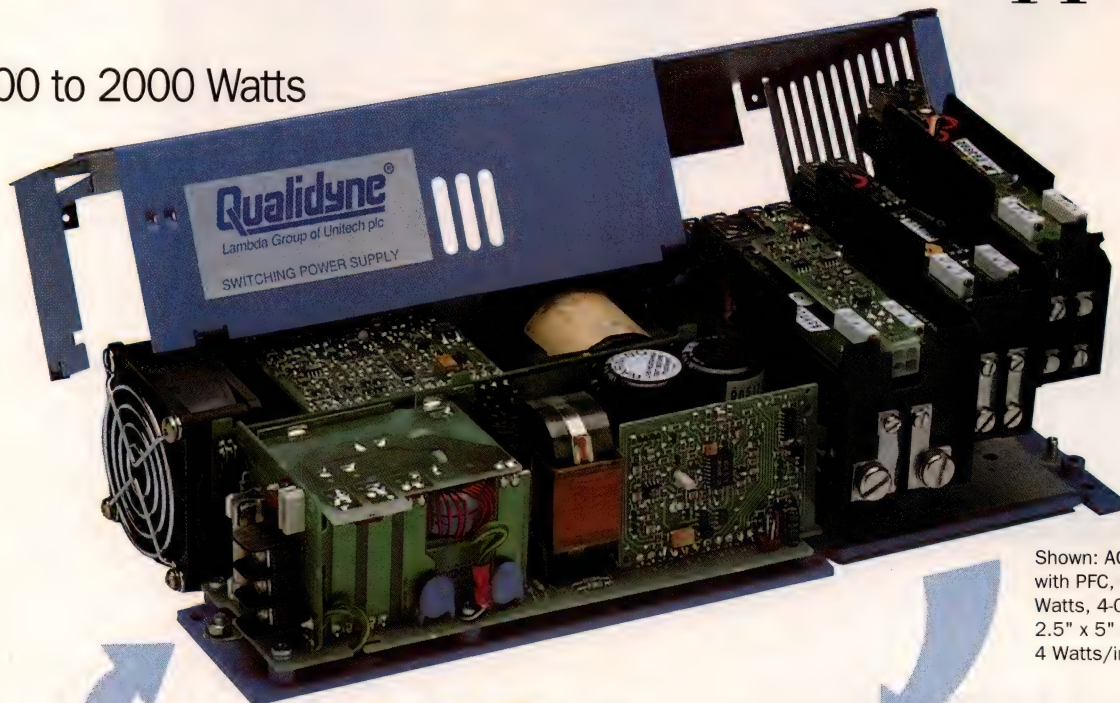
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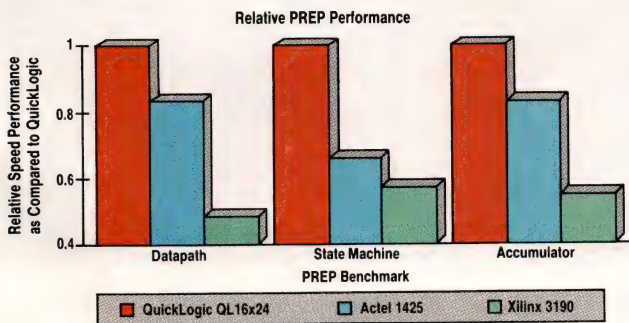
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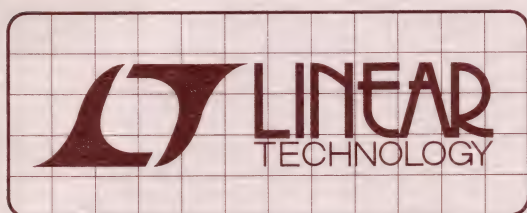
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# DESIGN NOTES

## Triple Output 3.3V, 5V, and 12V High Efficiency Notebook Power Supply – Design Note 78

Randy G. Flatness

The new LTC1142 is a dual 5V and 3.3V synchronous step-down switching regulator controller featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. Two independent regulator sections, each driving a pair of complementary MOSFETs, may be shut down separately to less than 20μA/output. This feature is an absolute necessity to maximize battery life in portable applications. Additionally, the input voltage to each regulator section can be individually connected to different potentials (20V maximum) allowing a wide range of novel applications.

The operating current levels for both regulator sections are user programmable, via external current sense resistors, to set current limit. A wide input voltage range for the LTC1142 allows operation from 4V to 16V. The LTC1142HV extends this voltage range to 20V, permitting operation with up to 12-cell battery packs.

Both regulator blocks in the LTC1142 and LTC1142HV use a constant off-time current mode architectures with Burst Mode™ operation. This results in a power supply that has very high efficiency over a wide load current range, fast transient response, and very low dropout. The LTC1142 is ideal for applications requiring 5V and 3.3V output voltages with high conversion efficiencies over a wide load current range in a small amount of board space.

The application circuit in Figure 2 is configured to provide output voltages of 3.3V, 5V, and 12V. The current capability of both the 3.3V and 5V outputs is 2A (2.5A peak). The logic controlled 12V output can provide 150mA (200mA peak), which is ideal for flash memory applications. The operating efficiency shown in Figure 1 exceeds 90% for both the 3.3V and 5V sections.

The 3.3V section of the circuit in Figure 2 is comprised of the main switch Q4, synchronous switch Q5, inductor L1, and current shunt  $R_{SENSE3}$ . The current sense resistor

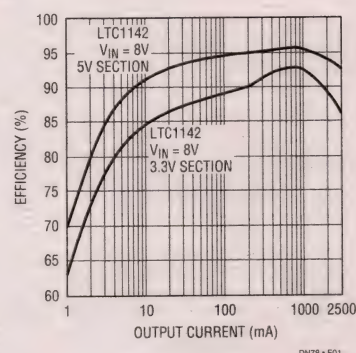


Figure 1. LTC1142 Efficiency

$R_{SENSE}$  monitors the inductor current and is used to set the output current according to the formula  $I_{OUT} = 100mV / R_{SENSE}$ . Advantages of current control include excellent line and load transient rejection, inherent short-circuit protection and controlled start-up currents. Peak inductor currents for L1 and T1 of the circuit in Figure 2 are limited to  $150mV / R_{SENSE}$  or 3.0A and 3.75A respectively.

When the output current for either regulator section drops below approximately  $15mV / R_{SENSE}$ , that section automatically enters Burst Mode™ operation to reduce switching losses. In this mode the LTC1142 holds both MOSFETs off and sleeps at 160μA supply current while the output capacitor supports the load. When the output capacitor discharges 50mV, the LTC1142 briefly turns this section back on, or "bursts" to recharge the output capacitor. The timing capacitor pins, which go to 0V during the sleep interval, can be monitored with an oscilloscope to observe burst action. As the load current is decreased the circuit will burst less and less frequently.

The timing capacitors  $C_{T3}$  and  $C_{T5}$  set the off-time according to the formula  $t_{OFF} = 1.3 \times 10^4 \times C_T$ . The constant off-time architecture maintains a constant ripple current while the operating frequency varies with input voltage. The



3.3V section has an off-time of approximately 5 $\mu$ s resulting in a operating frequency of 120kHz at 8V input voltage. The 5V section has an off-time of 3.5 $\mu$ s and a switching frequency of 107kHz at 8V input voltage.

The operation of the 5V section is identical to the 3.3V section with inductor L1 replaced by transformer T1. The 12V output voltage is derived from an auxiliary winding on the 5V inductor T1. The output from this additional winding is rectified by diode D3 and applied to the input of an LT1121 regulator. The 12V output voltage is set by resistors R3 and R4. A turns ratio of 1:1.8 is used for T1 to ensure that the input voltage to the LT1121 is high enough to keep the regulator out of dropout while maximizing efficiency.

The LTC1142 synchronous switch removes the normal limitation that power must be drawn from the primary 5V

inductor winding in order to extract power from the auxiliary winding. With synchronous switching the auxiliary 12V output may be loaded without regard to the 5V primary output load providing that the loop remains in continuous mode operation.

When the 12V output is activated by a TTL high (6V maximum) on the 12V enable line, the 5V section of the LTC1142 is forced into continuous mode. A resistor divider composed of R1, R5 and switch Q1 forces an offset subtracting from the internal 25mV offset at pin 14. When this external offset cancels the built-in 25mV offset Burst Mode™ operation is inhibited.

For additional high efficiency circuits see Application Note 54.

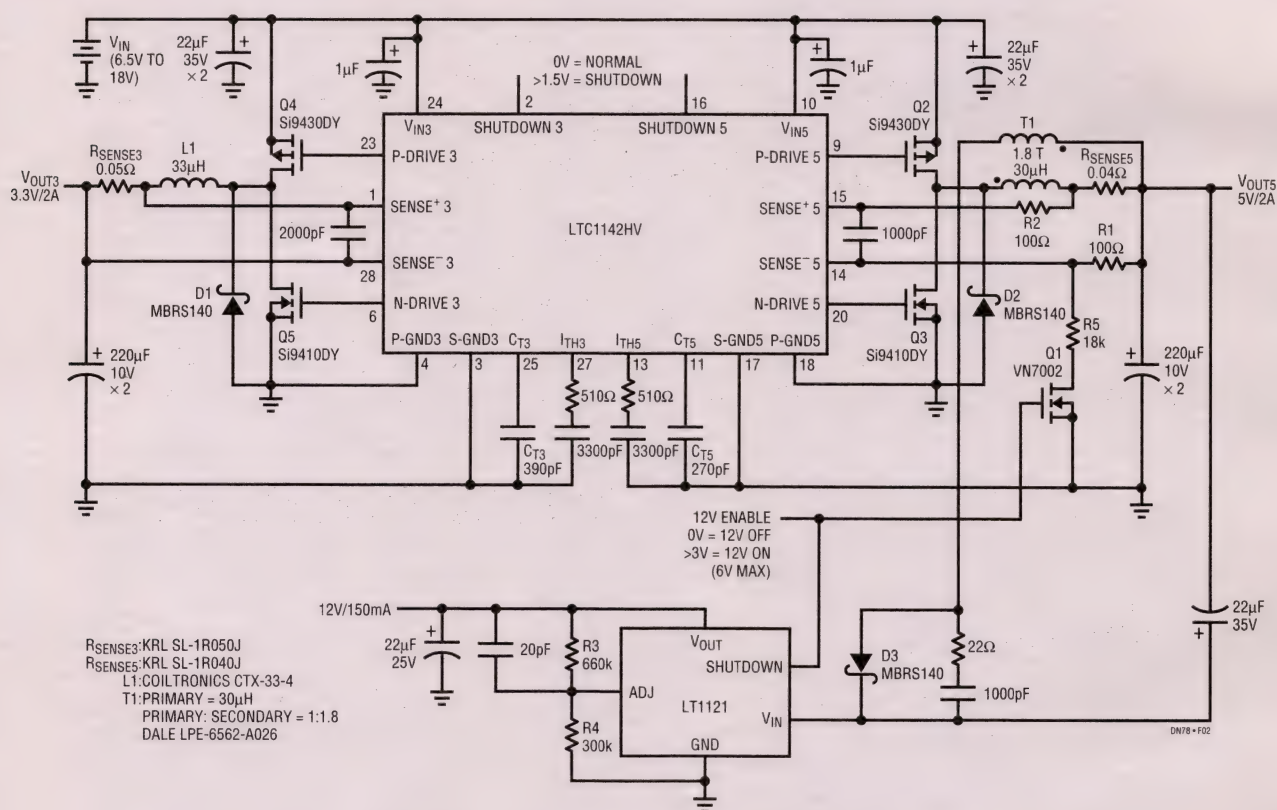


Figure 2. LTC1142 Triple Output High Efficiency Power Supply

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## Pulse stretcher increases ECL-gate gains

Nicholas J Bucska, PC Peripherals, Louisville, CO

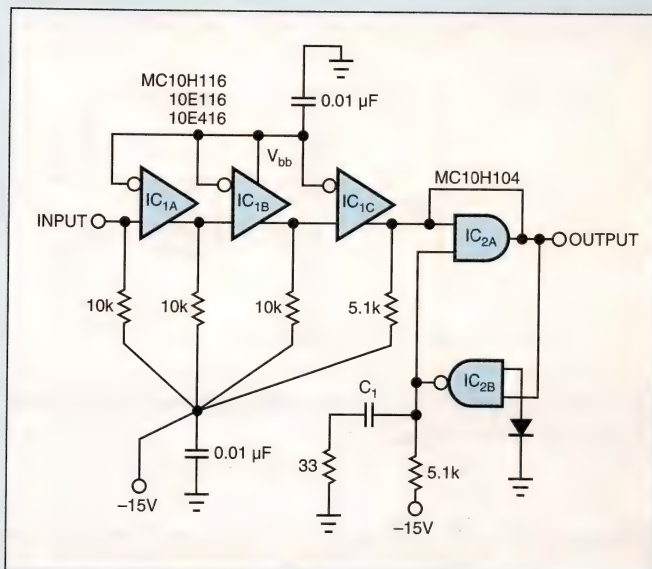
The circuit in **Fig 1** stretches the output pulses of an ECL comparator by operating the ECL line receivers with unusually large pulldown resistors to the  $-15\text{V}$  supply. The large load resistance maximizes the gains of the emitter-follower output stages and speeds up the rising edges. At the same time, the low pulldown current, together with the input and wiring capacitances, slows the falling edges. These actions stretch the positive pulses by approximately 2 nsec/stage.

ECL comparators usually have low gains, typically about 500. The receivers of  $\text{IC}_1$  increase this gain by a minimum of 60 to 100 times.  $\text{IC}_2$  is an unusual single shot, which stretches only the short pulses but leaves the long pulses unchanged. The circuit wire ORs the input of  $\text{IC}_{2A}$  to its output, so when the input goes high, it instantly pulls up the output. After one gate delay, the output of  $\text{IC}_{2A}$  becomes active and pulls the input up, latching it into high position. Now the output of  $\text{IC}_{2B}$  turns off, and its output drops with the slope determined by  $C_1$  and the pulldown current. After crossing the switching threshold,  $\text{IC}_{2B}$  turns off  $\text{IC}_{2A}$ , which resets the latch. If the input pulse is longer than this delay, the latch has no effect.

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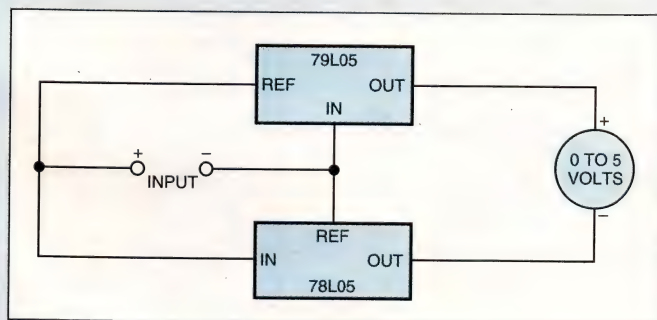


**Fig 1**—The circuit stretches the output pulses of an ECL comparator by operating the ECL line receivers with unusually large pulldown resistors.

## Expanded-scale voltmeter uses just two parts

DD Cantrell, North Valley Research, Los Molinos, CA

The expanded voltmeter in **Fig 1** doesn't require trimpots to obtain usable accuracy or require the tedious selection of Zener diodes. This circuit consists of only two parts and a 5V meter. The circuit is completely linear and requires no calibration except the rare mechanical zeroing of the meter. By using a split-voltage reference system with floating output, the zero point of the voltage supplied to the meter equals the absolute sum of the two references. With the regulators in



**Fig 1**—Using a split voltage-reference system with floating output, the zero point of this expanded-scale meter equals the absolute sum of the two references.

the **figure**, the 0 to 5V meter reads 10 to 15V inputs. If the voltage into the system falls below this level, the output to the meter changes polarity. This feature allows use of the mechanical zeroing of the meter, although this zeroing should never be necessary because most regulators yield outputs more accurate than the meter can read.

The pinouts of these TO-92 devices are perfect for this application. The small size allows installation of the circuit within most meter cases. Keep in mind that this circuit will present a load of 3 to 5 mA, and connections should minimize any voltage drops between meter and battery.

For use with other voltages, select regulators for sums equaling the lowest voltage to be displayed. As an example, a 78L15 and a 79L05 will output a zero voltage at 20V. A 5V meter will then read from 20 to 25V. You can make the circuit adjustable by substituting a 317L adjustable regulator and the necessary resistors in place of the 78L05.

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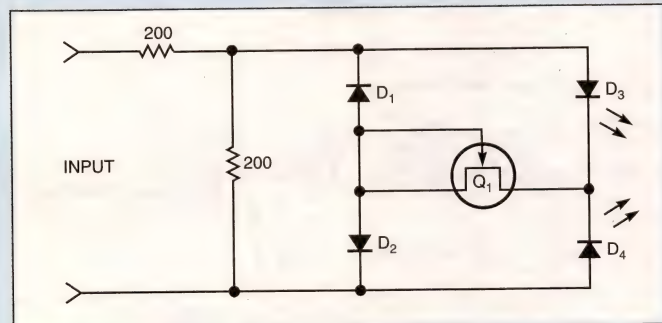
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## Simple circuit detects current pulses

Richard McGillivray, Grey Bruce Regional Health Centre, Owen Sound, Ontario, Canada

The pulse detector in **Fig 1** provides a visible indication of positive and negative current pulses. The pulses' amplitudes can vary from 20 to 150 mA. The pulses' durations can range



**Fig 1**—This pulse detector provides a visible indication of positive and negative current pulses.

from 10 to 40 msec, and their repetition rate can span 40 to 180 pulses/minute.

In **Fig 1**, the junction of the resistive divider connects to a bridge rectifier comprising diodes  $D_1$  and  $D_2$ , and the LEDs  $D_3$  and  $D_4$ . An N-channel JFET,  $Q_1$ , is the load for the bridge. The JFET provides a constant-current sink for the LEDs. Obviously, the JFET must have an  $I_{DSS}$  of less than the maximum LED forward current.

$D_3$  and  $D_4$  indicate positive and negative pulses, respectively. The LEDs' brightness remains virtually constant over the specified range of input-current pulses.

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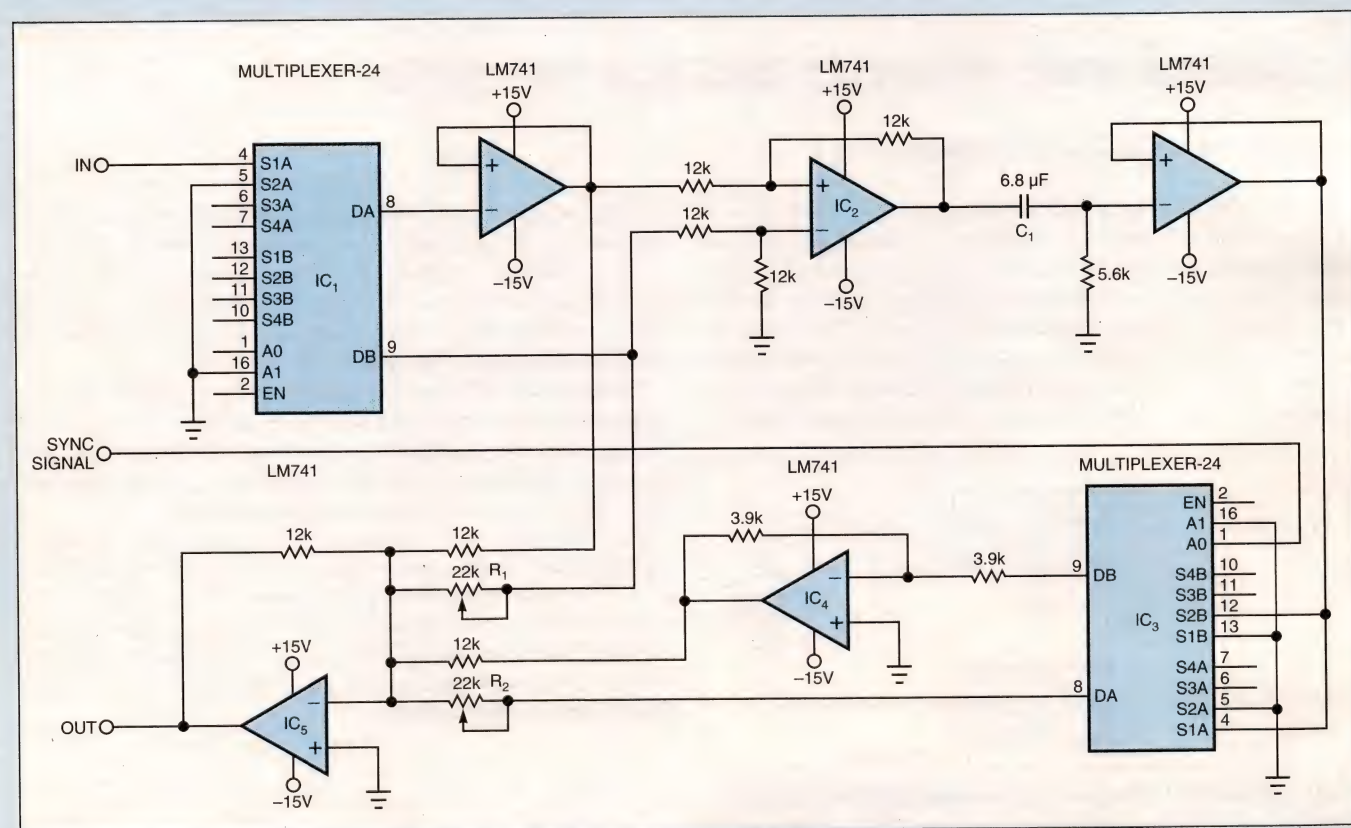
## Circuit eliminates hum from pulsed signal

Stanislav Tomek, Slovak Technical University, Slovak Republic

The circuit in **Fig 1** eliminates hum from a periodic signal by a factor of as much as 100:1. **Fig 2a** shows an incoming signal that combines a periodic square wave and a much lower fre-

quency hum. Suppose for simplicity's sake that the hum is sinusoidal.

The input signal has two envelopes that follow the hum



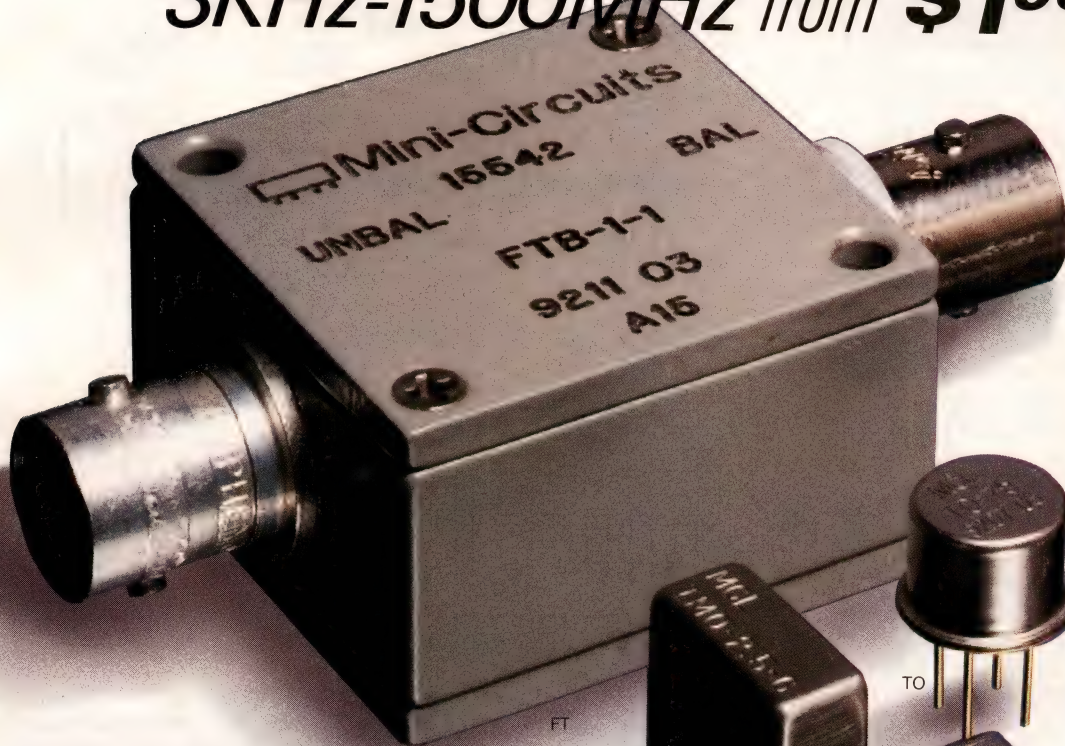
**Fig 1**—This circuit eliminates hum from a periodic signal by a factor of as much as 100:1.



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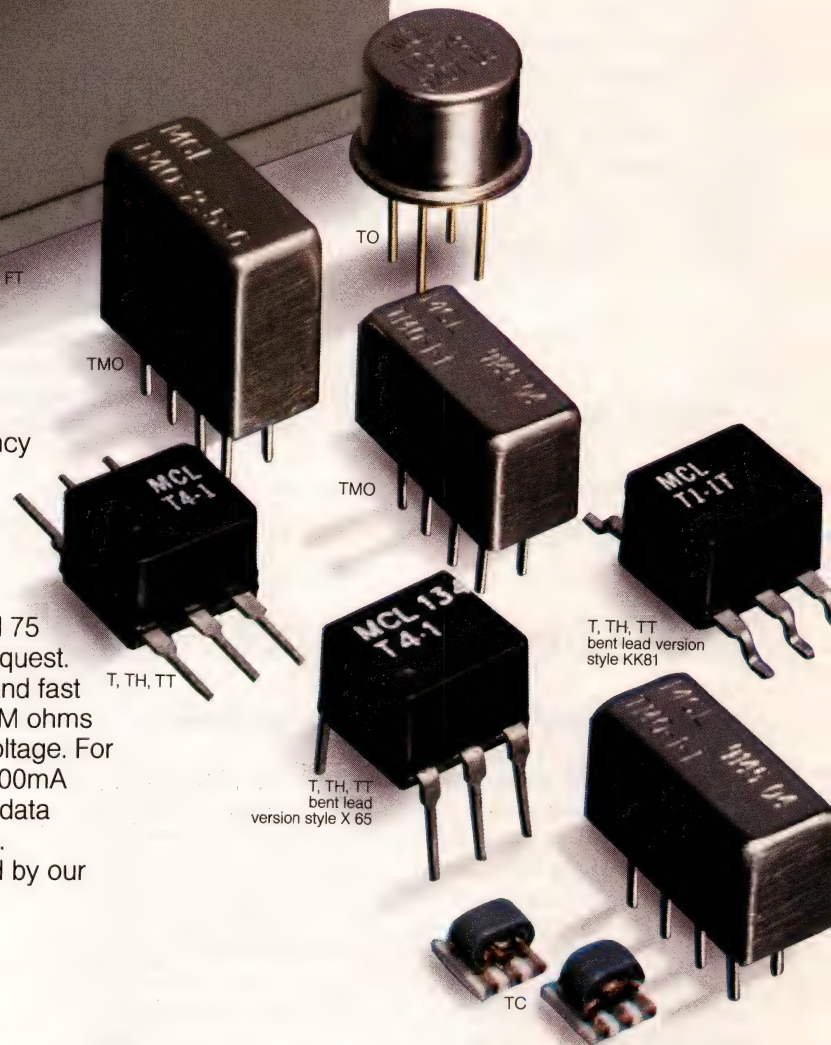
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(Fig 2a). The circuit separates these two envelopes and then subtracts them, yielding the waveform in Fig 2b. This signal has an ac and a dc component. A capacitor eliminates the dc component, and the circuit splits the signal into the waveforms in 2c and 2d, inverting negative excursions to get the signal in 2c.

Notice that the sum of Fig 2c and Fig 2d is the inverse of the hum. Therefore, summing Fig 2a with Fig 2c and Fig 2d yields the reconstructed pulse signal in Fig 2e.

The analog multiplexer, IC<sub>1</sub>, in Fig 1 separates the signal envelopes. The op amp IC<sub>2</sub> subtracts them from each other. The capacitor C<sub>1</sub> removes the dc level from the signal. The analog multiplexer IC<sub>3</sub> divides the signal into positive and negative parts. The inverter IC<sub>4</sub> inverts the negative part of the signal. Op amp IC<sub>5</sub> sums the signals to derive the output.

The external signal, which has the same frequency and phase as the pulse signal, synchronizes the analog multiplexers. Trimmers R<sub>1</sub> and R<sub>2</sub> optimize performance. EDN BBS /DI\_SIG #1352

EDN

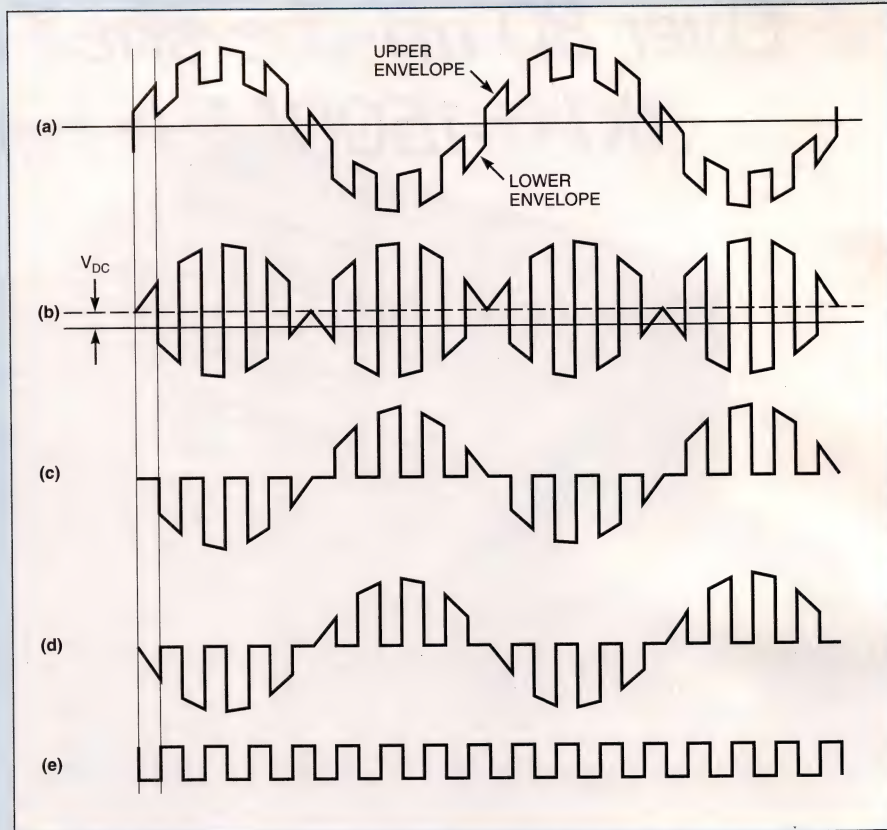


Fig 2—2a shows an incoming signal, which combines a periodic square wave and a much lower frequency hum. The input signal has two envelopes that follow the hum. The circuit separates these two envelopes and then subtracts them, yielding the waveform in 2b. A capacitor eliminates 2b's dc component, and the circuit splits the signal into the waveforms in 2c and 2d (inverting negative excursions to get the signal in 2c). Summing 2a with Fig 2c and Fig 2d yields the reconstructed pulse signal of 2e.

To Vote For This Design, Circle No. 375

## MOSFET replaces switch

Malcolm Watts, Wellington Polytechnic, Wellington, New Zealand

By using a cheap, readily available MOSFET, you can use a single-pole switch to turn a bipolar power supply on and off without consuming extra power. In Fig 1, the switch simply controls the MOSFET gate, which switches on the negative supply. Resistor R, which can be several megohms, is not necessary if the  $\pm 6V$  rails are permanently connected to a load, such as an op-amp circuit. Because the MOSFET's  $R_{DS(ON)}$  is a fraction of an ohm, power loss is minimal, and the circuit suits moderate-consumption, battery-operated circuitry. EDN BBS /DI\_SIG #1360

EDN

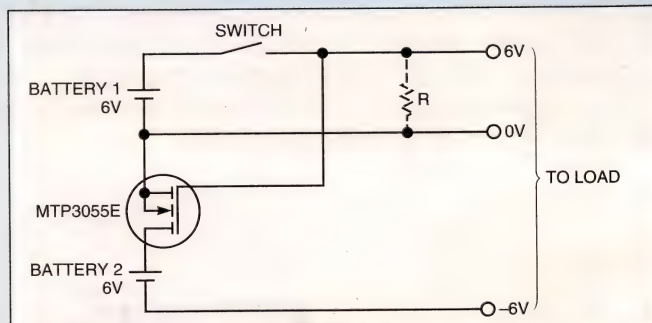


Fig 1—The switch simply controls this circuit's MOSFET gate to turn the negative supply on and off.

To Vote For This Design, Circle No. 376

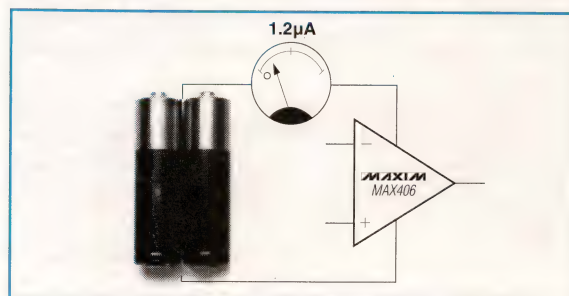


# 1.2 $\mu$ A SINGLE SUPPLY OP AMPS SWING RAIL-TO-RAIL

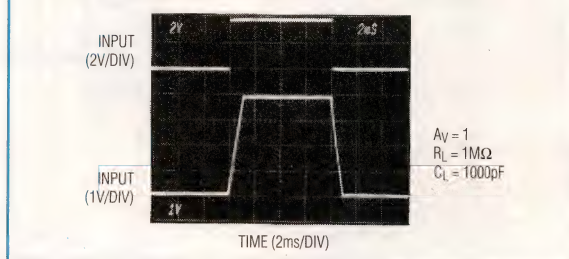
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MAX406	Single	1.2	500 $\mu$ V	40	GND to +3.9V	YES	8-DIP/SO
MAX409	Single	1.2	500 $\mu$ V	150 (A <sub>V</sub> $\geq$ 10V/V)	GND to +3.9V	YES	8-DIP/SO
MAX407	Dual	1.2	3	8	GND to +3.8V	YES	8-DIP/SO
MAX417	Dual	1.2	3	150 (A <sub>V</sub> $\geq$ 10V/V)	GND to +3.8V	YES	8-DIP/SO
MAX418	Quad	1.2	3	8	GND to +3.8V	YES	14-DIP/SO
MAX419	Quad	1.2	3	150 (A <sub>V</sub> $\geq$ 10V/V)	GND to +3.8V	YES	14-DIP/SO



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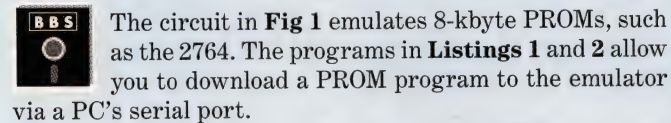
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## PC programs PROM simulator

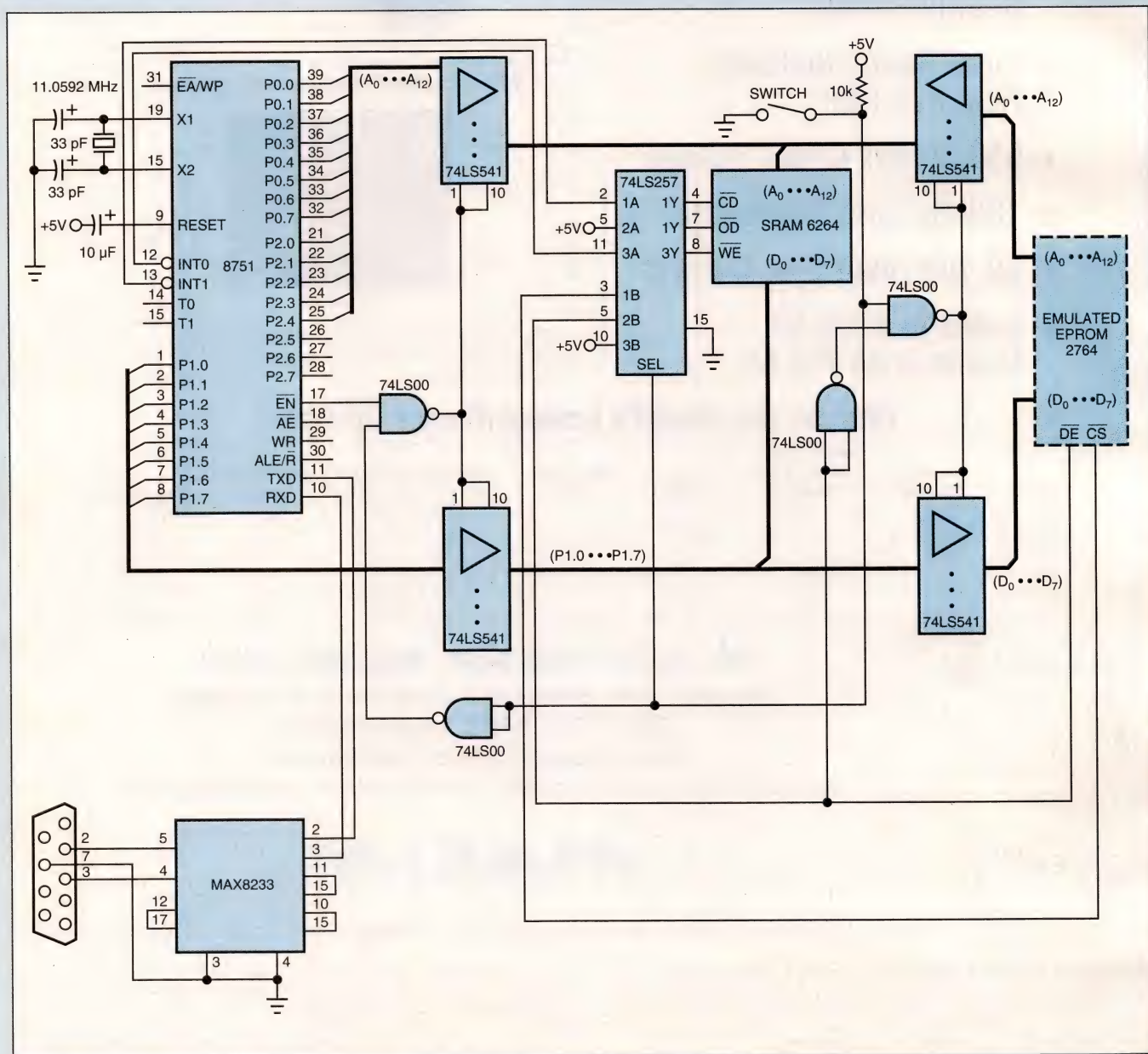
**Shwang-Shi Bai, Chang-Shan Institute of Technology, Taiwan, ROC**



To operate the emulator, you first set the SPST switch to the closed, or down, position. The PC then downloads the PROM's data via the emulator's 8751 microcontroller. Moving the switch back to the open position puts the circuit in emulation mode.

The compressed ZIPfile, DI1346Z.ZIP, attached to the message /DI\_SIG #1346, contains **Listings 1** and **2** as well as executable files and an OrCAD 2.0 version of the schematic in **Fig 1. EDN BBS /DI\_SIG #1346**

**To Vote For This Design, Circle No. 377**



**Fig 1—The 8751 microcontroller in this circuit accepts PROM programs from a PC's serial port, loading them into onboard SRAM, so that the circuit can emulate 8-kbyte PROMs.**

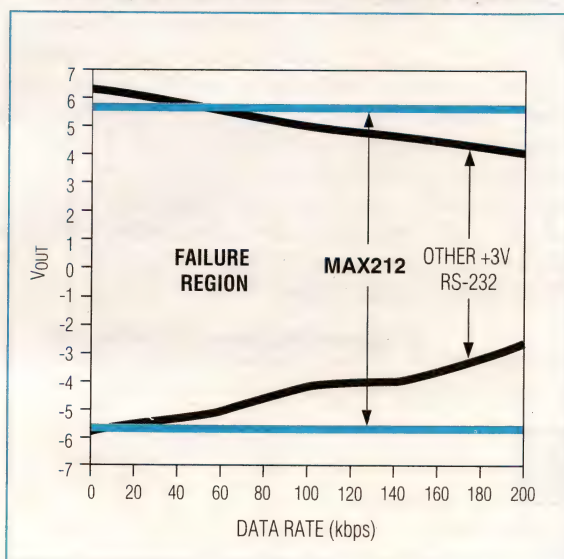


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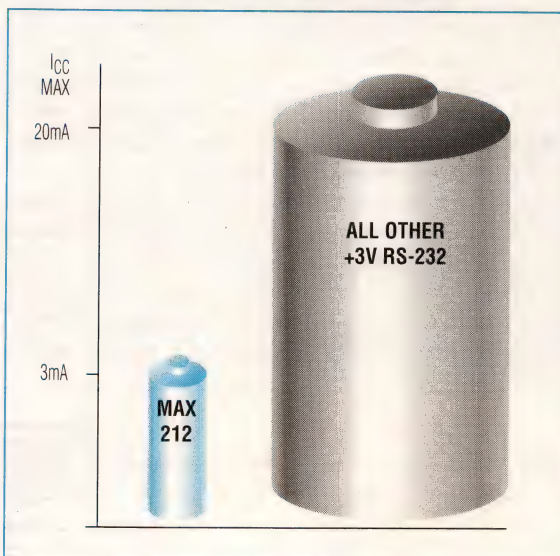
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# Status indicator flags five discharge states

Glen Chenier, Fitel Photomatrix, Nepean, ON, Canada

With just one leftover op amp or comparator, you can add a battery-condition indicator to your portable circuit design. To indicate the life in an aging battery visually, the circuit in **Fig 1** varies the duty cycle and flash rate of an LED when the battery voltage drops below established limits.

The circuit actually indicates five conditions of the battery. A steady glow assures the user that the battery is strong and healthy. A 2-Hz brief flicker off indicates that the battery is starting to show age. A more insistent, 50%, 5-Hz flashing is a warning to have a spare battery on hand. A brief flicker on at 2 Hz is the battery's last gasp. And, when the LED is continuously off, it's time to replace the battery.

The component values in the **figure** switch the LED from steadily on to flash mode when the 9V battery drops to about 6.5V and the LED is continuously off below 5.5V. You can tweak the resistor values for different voltage thresholds as desired.

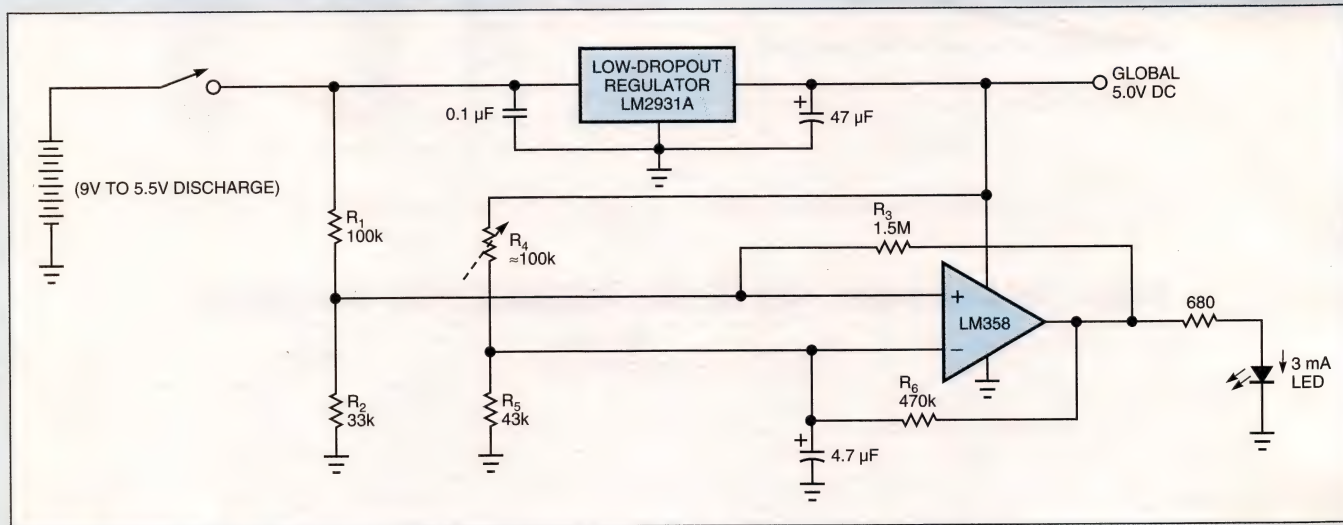
The circuit holds the op amp's minus-input voltage between the upper and lower limit that  $R_4$ ,  $R_5$ , and  $R_6$  estab-

lish. For a precise dead-battery threshold, make  $R_4$  adjustable to offset the variations in regulator tolerance. The circuit oscillates only when the battery-sense voltage at the op amp's plus input is within those limits. Above and below these limits, the circuit functions as a comparator and holds the LED continuously on or off. Within the limits, the capacitor sawtooth will have the amplitude established by the hysteresis of  $R_1$ ,  $R_2$ , and  $R_3$ . The hysteresis must be smaller than the capacitor-sawtooth limits, and their difference defines the voltage range over which the circuit oscillates. Calculations are tedious, so you'll find it easier just to breadboard the circuit and tickle the values until the circuit percolates at the thresholds you want. An LM358 can drive a high-efficiency LED, but higher current requirements or open-collector comparators need a buffer transistor.

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**Fig 1**—Depending on the status of this indicator circuit's 9V battery, the op amp either keeps the LED continuously on or off, or the circuit oscillates to alert you to three additional stages of battery discharge.

## ADC helps temperature-compensate transducer

Alexander L Belousov, Science Instruments Co, Baltimore, MD

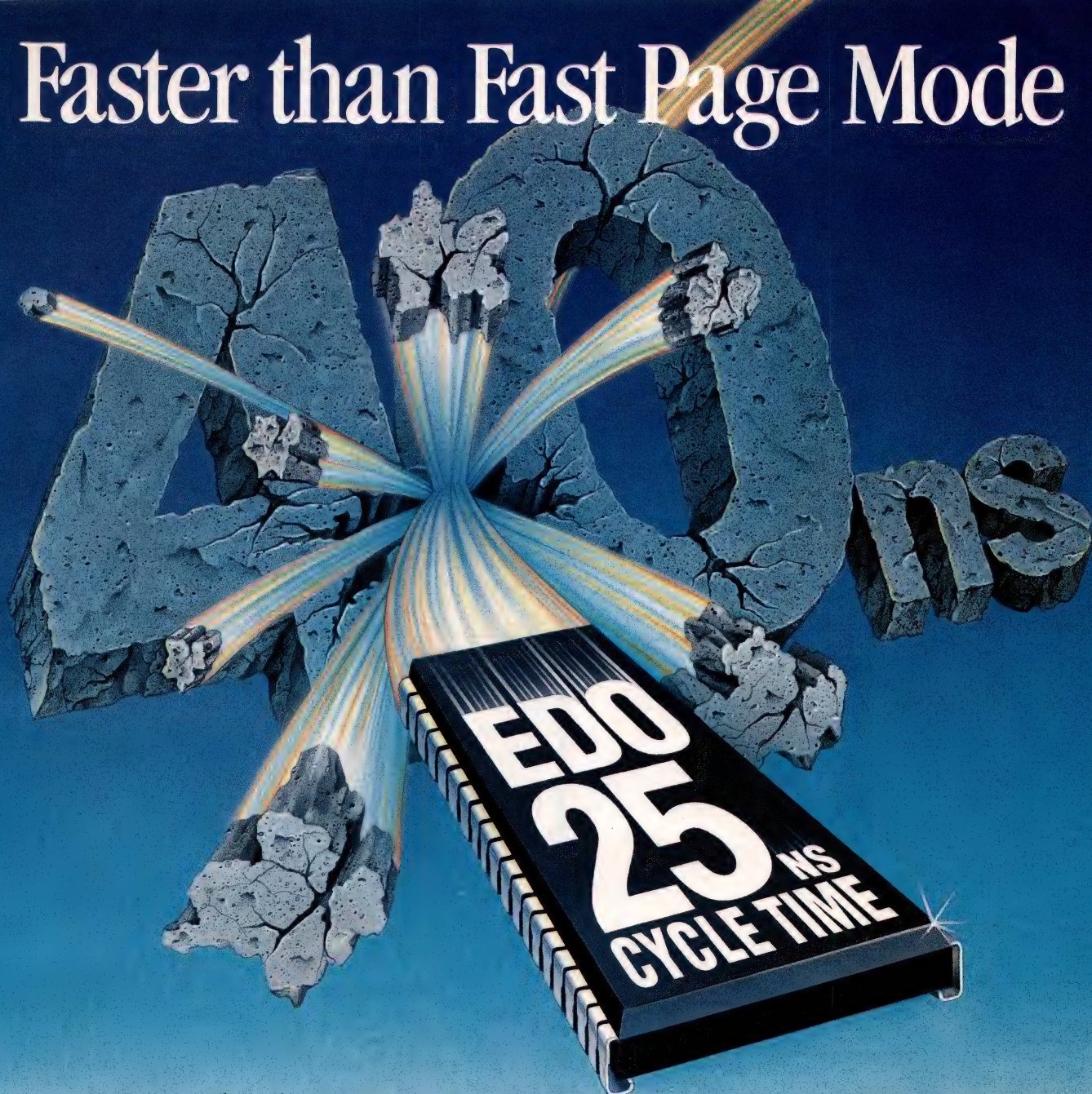
You can use many tricks to make temperature-compensated resistive full-bridge transducers, such as piezoresistive pressure or strain-gauge sensors. Most of these tricks use some additional thermosensitive components that produce a compensating voltage or current. The disadvantages of such solutions are obvious: low accuracy due to the inevitable temperature difference between the sensor's body and resistive bridge, increased circuit complexity due to the extra parts, and demands for accurate adjustment of analog values.

The alternative in **Fig 1** uses an ADC and takes advantage of the thermal properties of resistive solid-state sensors such as pressure sensors or strain gauges. Without any additional temperature-sensitive components, the output of the circuit, which is in a form of a digital code, includes the temperature compensation. This technique is applicable to all full-bridge resistive sensors.

The equivalent resistance of the full-bridge pressure sensor depends on the temperature and, for a first approxima-



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MT4LC4007J	4 Meg	1 Meg x 4	60/25, 70/30	Now/2Q94
MT4C16270	4 Meg	256K x 16	60/25, 70/30	Now
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## EDN-DESIGN IDEAS

tion, is independent of the pressure. If you apply a constant voltage to the bridge, the current will be inversely proportional to the bridge's resistance, and the current's sign will be the inverse of the temperature effect in comparison with the bridge's resistance. The op amp will produce an output voltage proportional to the full bridge current and the resistance of  $R_{FB}$ . The circuit applies this voltage, which includes the temperature effect, to the reference pin of the ADC and applies the sensor's output to the ADC's differential input.

Most solid-state pressure sensors have negative temperature coefficient of span (TCS) and positive temperature coefficient of resistance (TCR). The absolute values of TCS and TCR are very close to each other. For example, the SLP004D from SenSym Inc (Sunnyvale, CA) has typical values of TCS equal to  $-2400 \text{ ppm}/^\circ\text{C}$  and TCR of  $+2300 \text{ ppm}/^\circ\text{C}$ . The MPX-50, -100, and -200 pressure sensors from Motorola (Phoenix, AZ) have typical values of TCS equal to  $-0.19\%/^\circ\text{C}$  and TCR of  $+0.24\%/^\circ\text{C}$ . So, the output voltage of  $IC_1$  will have negative temperature coefficient very close to the TCS of the sensor.

The ADC provides the perfect opportunity to output, in the form of a digital code, a precise ratio of two analog signals applied to the ADC's input and reference pins. So, the analog-to-digital conversion reduces the total TCS of the transducer to approximately the algebraic sum of TCS+TCR.

The inverting input of the op amp connects to ground, so the sensor will operate exactly as if it were really grounded except for the error introduced by the input offset voltage and current of the op amp. In most modern op amps, this error is negligible when you compare it to the commonly 5 or 10V  $V_{REF}$  applied to sensor. Note that the TCR of  $R_{FB}$  also affects the total TCS. For better compensation, it is possible to use a feedback resistor with small TCR approximately equal to TCS+TCR and locate the resistor as close to the sensor as possible.

Although this circuit uses an ADC from National Semiconductor's (Santa Clara, CA) ADC0801 to ADC0805 family, many others will also work. For single-ended ADCs, you can add any differential amplifier, such as Analog Devices' (Wilmington, MA) AD620. Many op amps will also work with this technique, and the choice of both ADC and op amp depends on the required accuracy.

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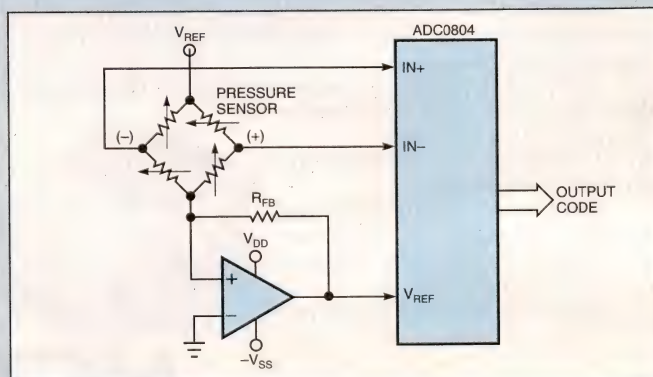
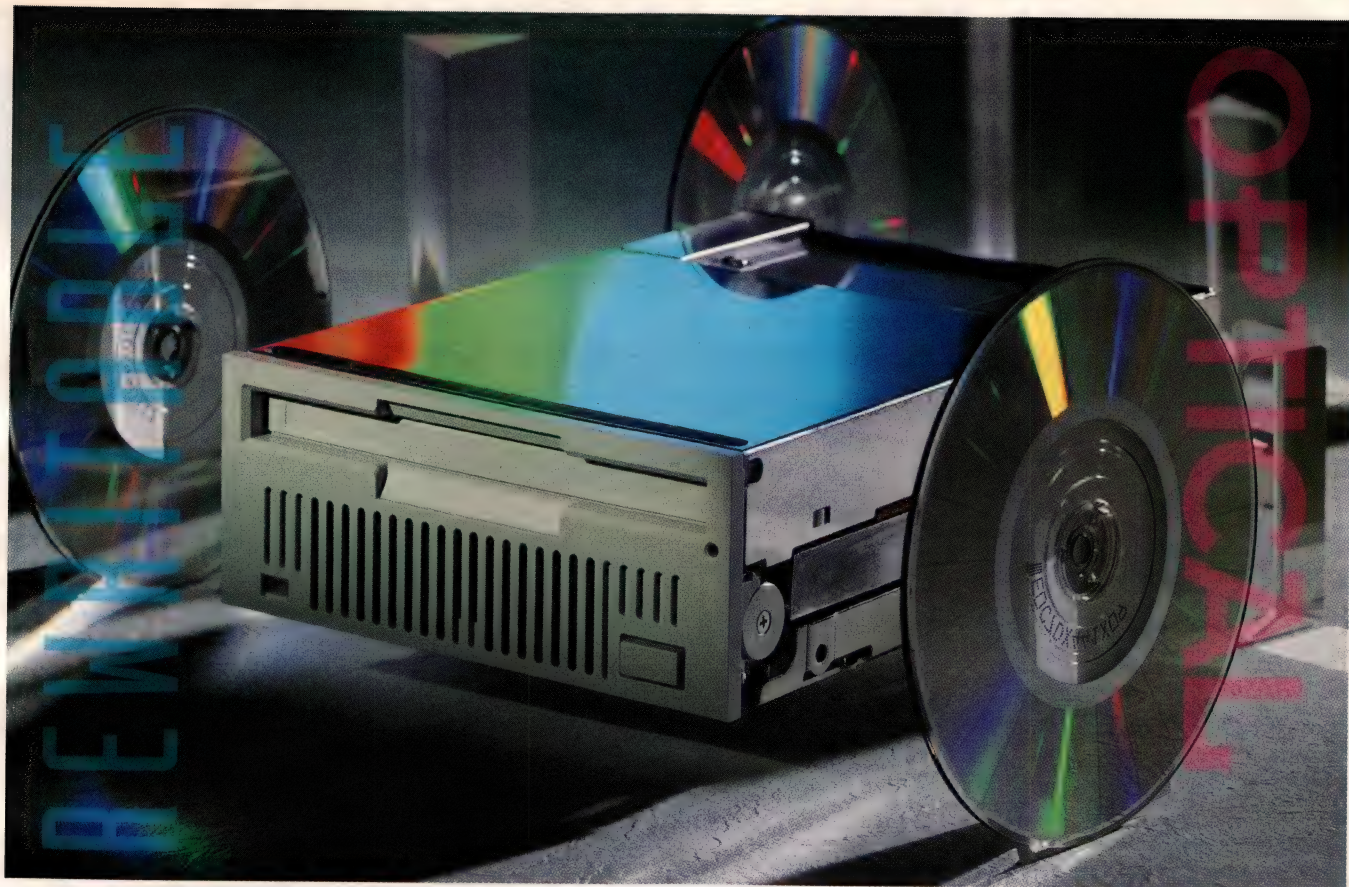


Fig 1—Applying a voltage proportional to a sensor's current, which includes temperature effects to the reference input of an ADC, produces a temperature-compensated digital output.





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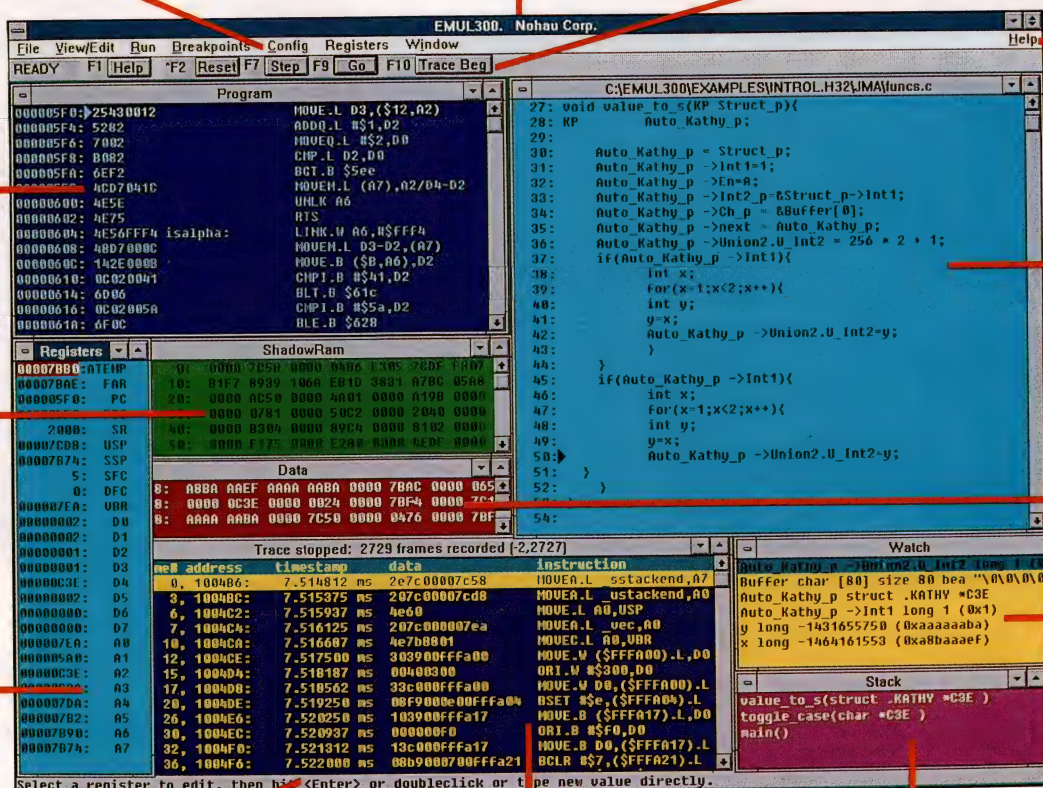
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EMBEDDED SYSTEMS, David Shear, Technical Editor

## I want to know less!

It seems that most of the new methodologies that come along each year require that you know more than you do now. The structured methodologies of the 1980s required that you first know how to write programs and, second, that you understand and implement the methodology. Object-oriented programming of the 1990s similarly requires that you first have a deep understanding of a language, such as C, and then a knowledge of how to use the objects in C++.

Each year, someone comes up with something new that is not really new but just an extension of existing practices. The last real innovation was the move from assembly language to high-level language (HLL).

Moving from assembly language to an HLL allows you to know less to get your job done. You don't have to learn the architecture of the  $\mu$ P of the month. You don't have to worry about memory spaces and addresses. You can approach your problem from a signif-

icantly higher level of abstraction.

But as good as an HLL is, it is reaching the limits of its usefulness. I am tired of getting mired down in ridiculous details. Is it & or \*? How did I declare this pointer anyway? Why does the compiler allow me to use = when I should have used ==?

It is time for the tools to get out of the way. I know that there are plenty of people out there who are pleased with the status quo. They will be amazed that someone would make the accusation that existing tools are inadequate. They can get their jobs done; why can't I?

Well, I *can* get the job done, but only after wasting too much time. It angers me to have to stop thinking about a project to focus on mindless details. I know exactly what I want the embedded system to do. But I find myself wasting time trying to convince the C program I have written to do what I want.

Perhaps you are a better programmer. Perhaps you are nearly perfect and

haven't spent too much time debugging programs instead of working on projects. But if you have never experienced the waste of time debugging stupid problem causes, you have not done much real programming.

By "real" programming I mean programming in the real world—not "real-time" programming, which is writing a "program" that performs certain functions within limited time constraints. Real programming, on the other hand, is when *you* must perform certain functions within limited time constraints.

When doing real programming, you don't have the time to play with technology. You have a job to do, and these tools and languages are merely tools of the trade. There is no room for overdeveloped loyalties to the latest fad (reaching the point of religious fervor).

Anyway, I want to forget all that I know about programming and concentrate on the project. I want to develop code with the ease of developing digital logic

in the old 7400 days. In those days, you could look through a data book and select the circuit functions that you needed. Then you bought them off the shelf and plugged them together. You didn't have to spend so much time dealing with the technology. You could just select, plug, and play.

Imagine creating your embedded system by selecting proven functions from a pull-down menu and connecting them on your screen. You could keep sight of the project and use proven code that would work (or your money back).

You would not have to deal with the many details you now have to. You would have to *know less*. Packages that allow you to know less are beginning to show up, with more on the way this year.

Only when you have to know less to get the job done will you be able to make a large jump in productivity. Not only that, but the ease of use of these tools will make them more available to a wider audience.—David Shear

**Forth cross-compiler works on 68HC16.** The chipFORTH interactive cross-compiler is available for Motorola 68HC16-based projects. The device lets you develop code on a PC and use the chip's background-debug mode to debug the program. It includes a multi-tasking executive and development environment for the PC. The device also comes with the Motorola M68HC16Z1EVB evaluation board. \$2495. **Forth Inc.**, Manhattan Beach, CA. (310) 372-8493. **Circle No. 360**

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**Enhance debugging on Analog Devices' EZ-LAB.** The LAB+ debugger connects to the ROM sockets of Analog Devices' EZ-LAB or the ADSP-2101. It lets you download code, view and modify registers and memory, single step, set breakpoints, and run the

applications. It connects to EZ-LAB via a 60-pin connector and frees up both serial ports on the ADSP-2101. It is compatible with Analog Devices' development tools. \$295. **Hollis Electronics Co.**, Amherst, NH. (603) 598-4640.

**Circle No. 361**

**SBC includes video interface and iSBX ports.** The 20-MHz 80C186EB single-board computer (SBC) fits onto a 9×12-in. board. The device includes a



# EDN-New Products

## EMBEDDED SYSTEMS

video interface, two RS-232C/422/485 ports, four iSBX ports, a parallel port, and other I/O subsystems. It also includes a PCMCIA slot and an optional touchscreen. \$795. **PDI Corp**, Annapolis, MD. (410) 224-2130. **Circle No. 362**

**C3X emulator uses scan-path interface.** The Tiger TEM31 C3X emulator runs on a PC and connects to the scan-path port on Texas Instruments' TMS-320C3X DSP chips. A 12-pin connector



connects the emulator to the target. The hardware on the DSP chips allow you to control the processor and view and modi-

fy memory or internal registers. The emulator also comes with a C source-level debugger. \$3995. **DSP Research Inc**, Sunnyvale, CA. (408) 773-1042. **Circle No. 363**

**RTOS gives more power to the PowerPC.** The OS-9000 real-time operating system (RTOS) operates on the PowerPC 4xx and 6xx RISC processors. It uses the Atomic OS-9000 kernel and includes the Tool Kit and FasTrak development tools. The company has scheduled beta versions for the second quarter of this year. An OS-9000 Developer's Pak costs \$10,000. **Microware Systems Corp**, Des Moines, IA. (515) 224-1929. **Circle No. 364**

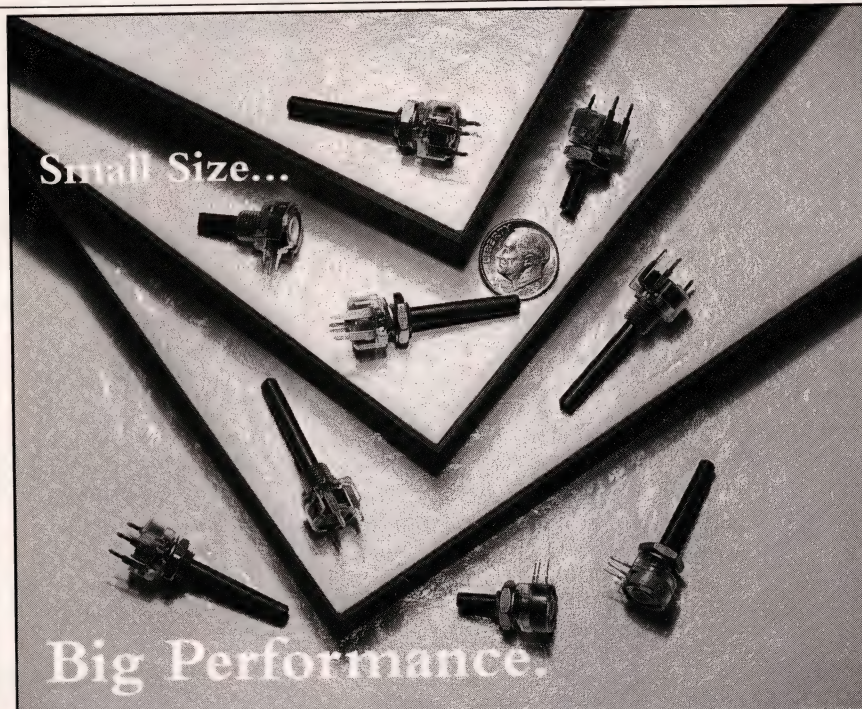
**ICE for 6800/2/9 and 68HC11 runs on PC.** The ET-ic6800 is a PC-based in-circuit emulator (ICE) that supports the 6800/2/9  $\mu$ P family and the 68HC11  $\mu$ C. It provides real-time emulation at speeds up to 4 MHz. The device comes with 64 kbytes of overlay RAM, 64 kbytes of breakpoint RAM, a source-level debugger, and a development environment. \$2715. **Emulation Technology Inc**, Santa Clara, CA. (408) 982-0660. **Circle No. 365**

**68306 ICE implements dual-processor pod.** The HMI-200 in-circuit emulator (ICE) for the Motorola 68306  $\mu$ P operates at up to 16 MHz. It has four complex breakpoints, two 4k $\times$ 80-bit trace buffers, and 256 kbytes to 4 Mbytes of overlay RAM. The pod contains two 68306  $\mu$ Ps to allow a more complete view into the program flow. The device also includes the SourceGate II source-level debugger. \$11,000. **Huntsville Microsystems Inc**, Huntsville, AL. (205) 881-6005. **Circle No. 366**

## REVISIONS

The latest version of Xray Masterworks includes source-code management, a Make utility, an upgraded version of the Xray debugger, and a graphical program analyzer. Prices start at \$8300. **Microtec Research Inc**, (408) 980-1300. **Circle No. 367**

COINS, an addition to the COSSAP DSP design-automation tool, allows you to write algorithms in C. The package then takes the C code and converts it to a model for simulation within COSSAP. **Cadis Software Ltd**, (415) 615-7789. **Circle No. 368**



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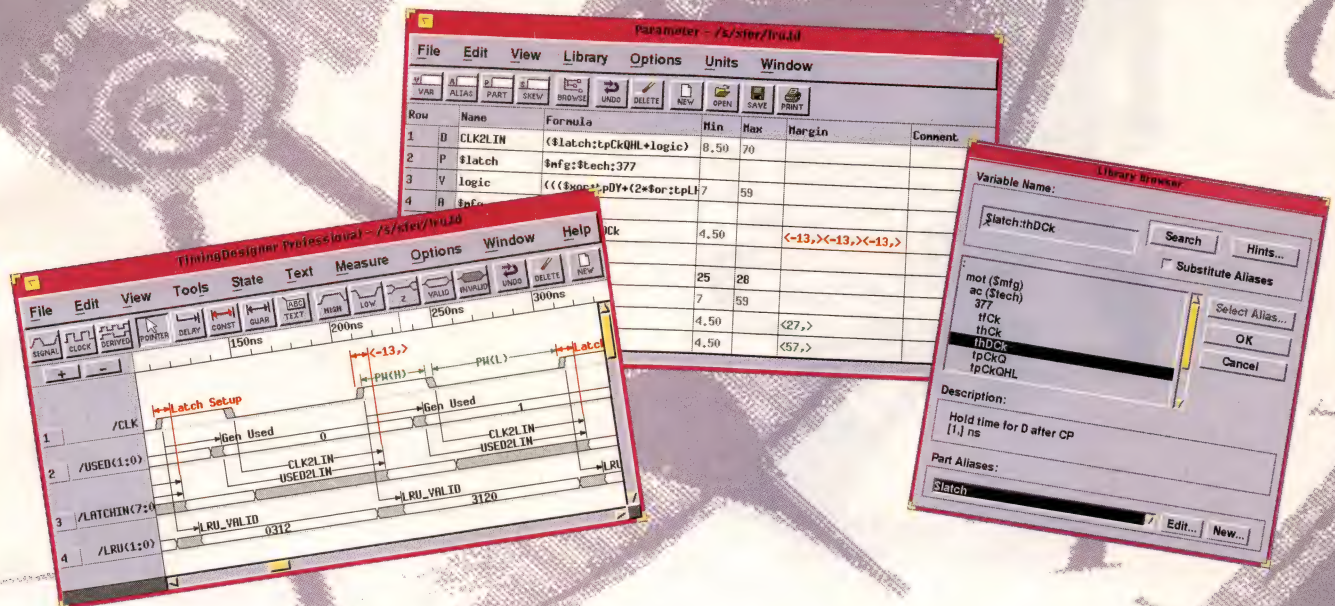
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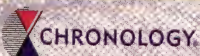


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CIRCLE NO. 75



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ACT 2 is not only fast, but predictably fast,

Chart I	Actel	Actel	Xilinx	Altera
Device	A1240A	A1240A-2	XC4005A-5	EPM7256-20
Capacity <sup>1</sup>	15.3	15.3	15.4	14.7
Performance <sup>2</sup>	36.3 MHz	48.4 MHz	35.0 MHz	45.3 MHz
Price <sup>3</sup>	\$68.80	\$96.30	\$138.70	\$214.25

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Chart II	Actel	AMD
Device	A1225A	22V10Q-25
# Devices	1	12
Total Icc Power <sup>4</sup>	10 mA	660 mA
Total Price <sup>5</sup>	\$42.50	\$77.16

For integrating 2500 gates use one Actel FPGA or 12 22V10s



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1. Average number of PREP instances, approximately 4000 gates or 20 PALCE22V10s. 2. PREP Derived Data-average internal operating frequency, in MHz.

3. 100 piece PQFP price quoted by authorized distributor, August/September 1993. 4. Typical Icc per device multiplied by number of devices.

5. Based on 100 piece PLCC price quoted by authorized distributor, August/September 1993. ACT, PLICE, Designer, and the Actel logo are trademarks or registered trademarks of Actel Corporation. PREP is a trademark of the Programmable Electronics Performance Corporation.

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 <b>PT5600/5700</b>	Dual 1 Amp	80%	<b>DUAL 1 AMP SWITCHER</b> <ul style="list-style-type: none"><li>• <math>V_o</math> of 3.3V/5V or 5V/12V</li><li>• Dual version of Standard 1 Amp Switcher</li></ul>
 <b>"78/79" SERIES</b>	1.5, 2, 3 Amp	85%	<b>78/79 SERIES</b> <ul style="list-style-type: none"><li>• <math>V_o</math> of 3.3V to 15V</li><li>• Pin-compatible with linear regulators</li><li>• Wide choice of output voltages and power levels</li></ul>
 <b>PT6100</b>	1, 2, 3 Amp	90%	<b>HIGH-PERFORMANCE, SUPER-EFFICIENT ISR</b> <ul style="list-style-type: none"><li>• <math>V_o</math> of 3.3V, 5V, 12V</li><li>• Adjustable output voltage</li><li>• On/off control</li><li>• Full function, high efficiency regulator for emanding applications</li></ul>

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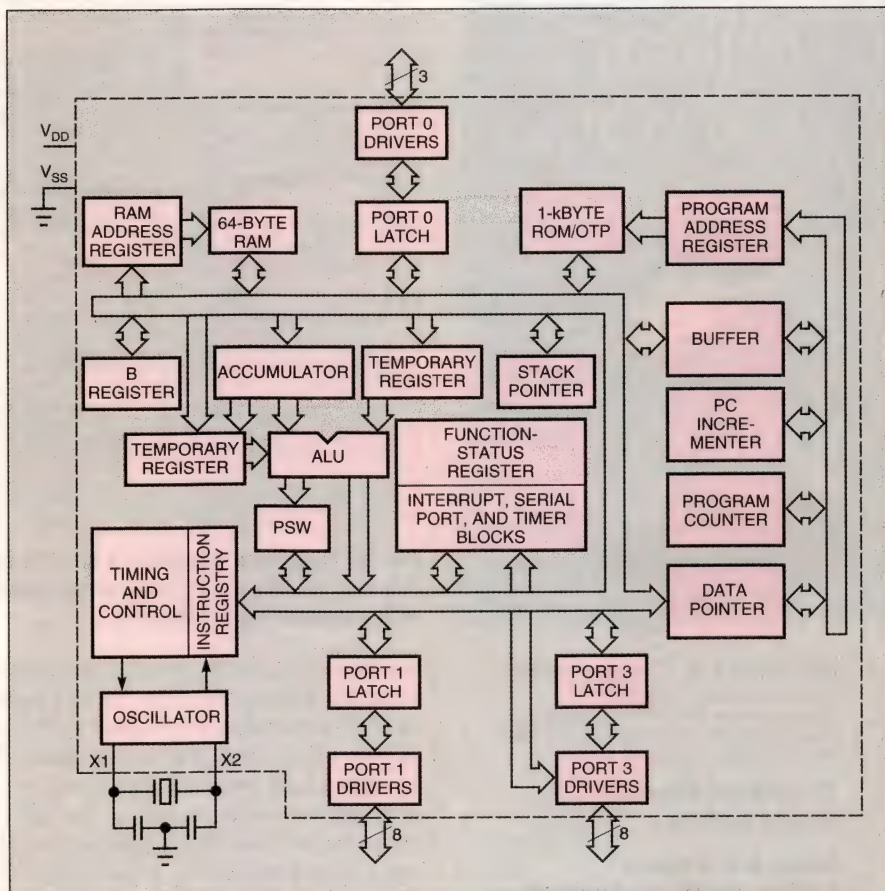
### Philips delivers one-two 8051 punch

Until now, the 8051 has not been a serious contender in the low-end 8-bit microcontroller world. Although ranking number two in the 8-bit  $\mu$ C market, it lacked a \$1 part for down-in-the-dirt applications. No more. Philips Semiconductors is introducing a stripped-down 83C750 and its more expensive OTP (one-time-programmable) companion, the 87C750. A descendant of the popular "skinny-DIP" 83C751, the new chip comes in at \$1 each (50,000).

The 83C750/83C750 integrates the 8051 core processor with 64 bytes of RAM and 1 kbyte of ROM or OTP. Using assembly language and this part, you can handle a range of low-end applications. Even better, you can prototype and do initial product builds with the OTP part, and when the design is stable, shift to lower cost ROM parts. Philips claims an 8-week cycle time for ROM-part delivery.

Clock rates run from 3.5 to 40 MHz. It executes a basic instruction cycle in 12 clock cycles. At 40 MHz, the CPU delivers 2- to 3-MIPS performance. Philips engineers trimmed back the standard 83C751 to get the cost-reduced controllers. For example, they reduced RAM and ROM and removed the serial I<sup>2</sup>C bus. The chip still has a 16-bit counter with automatic reloading capabilities to minimize overhead.

You can also get a low-cost, pseudo ICE (in-circuit emulator) to debug your code. As an introductory offer, Philips supplies a \$97.50 development tool from Ciebo. This tool emulates the 83C750/87C750  $\mu$ Cs with clock rates up to 40 MHz. Built around an 8052, the tool incorporates an in-memory monitor



**The 83C750/83C750 combines an 8051 processor with 64 bytes of RAM, 1 kbyte of ROM, and a 16-bit counter for low-end embedded applications. Clock rates reach 40 MHz.**

and a 64-kbyte trace buffer. It includes a source-code debugger for assembly, C, and PL/M languages. It also includes a 24-pin DIP emulation header and a programmer. —Ray Weiss

Philips Semiconductors, Sunnyvale, CA. (800) 447-1500. **Circle No. 369**

### Module eases Pentium design-in

Designing in a modern CPU chip such as the Pentium can be a tough chore, as faster clocks lead to tight timing and interface constraints. One way to minimize design time and eliminate potential errors is to rely on a processor/cache module—a module that integrates a CPU with a cache controller and a secondary cache. Integrated Business Computers offers such a short cut for Pentium mother-board

designers: PentiCache, a Pentium-based module. The module integrates the Pentium CPU with Intel's 82496 cache controller and 512 kbytes of zero-wait-state SRAM cache.

With the PentiCache module, you get a Pentium subsystem complete with a second-level, write-through cache. The module supports multiprocessing, with multiple PentiCache modules sharing a system memory. The module defines a system-memory-controller bus with up to 128 bits of data and 16 bits of parity. The interface to the memory controller is through two 160-pin, impedance-matched (50 $\Omega$ ), microstrip connectors. The interface can be asynchronous, synchronous, or strobed. A 10-pin header supplies JTAG access to the major-module components for onboard scan test.

The module supplies data and address parity checks for both the CPU

#### Philips 83C750/87C750 8-bit $\mu$ C

- 3.5- to 40-MHz clock
- 1-kbyte ROM/OTP (one-time programmable)
- 64-byte RAM
- 16-bit autoreloadable counter
- LED drive outputs
- 19 I/O pins
- Two external interrupts
- 16-byte encryption key, two security bits for OTP EPROM
- Idle and power-down modes
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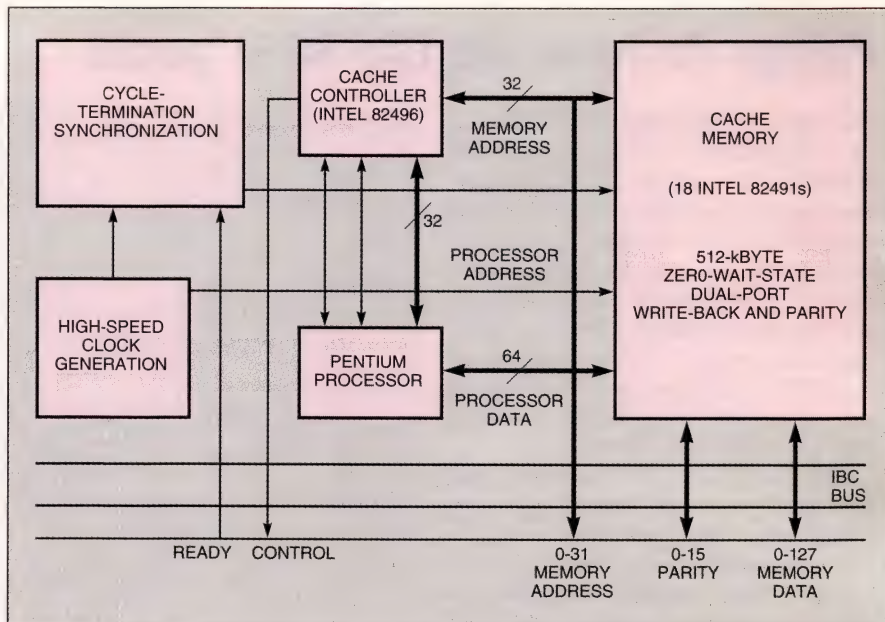
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CIRCLE NO. 31

94 • EDN January 20, 1994

## EDN-NEW PRODUCTS

### MICROPROCESSORS



The IBC PentiCache integrates a 60-/66-MHz Pentium CPU with an Intel cache-controller chip and 512 kbytes of 2-way set-associative cache. The modules support multiprocessing with a common system memory.

and memory buses, as well as snoop-memory addresses. The second-level cache incorporates write-back with the MESI (Modified Exclusive Shared Invalid) cache protocol. The 2-way set-associative cache includes the MRU (most recently used) hit-prediction and replacement algorithm. Read and write cycles have zero wait states for MRU hits and a 1-wait-state read for a read hit on an MRU miss. The module also includes a GaAs-based frequency synthesizer and a circuit synthesizer that supplies the module and the motherboard system clocks. —Ray Weiss

*Integrated Business Computers, Chatsworth, CA. (818) 882-8353.*

Circle No. 370

### IBC PentiCache module

- To 100-MHz clock
- 60- to 66-MHz Intel Pentium processor
- 512-kbyte write-back cache with parity
- 64- or 128-bit-wide system-memory bus with synch/asynch/strobed protocol
- Intel 82496 cache-controller chip
- 2-way set-associative cache with 32-, 64-, and 128-bit line sizes
- Zero-wait-state write hit cycles
- Concurrent CPU- and memory-bus cycles
- Supports JTAG test for all major-module chips
- MESI multiprocessor cache protocol
- 5.2x9.6-in., 8-layer pc board
- Prices vary based on Intel chip prices

## Book details Pentium architecture

Trying to learn a  $\mu$ P architecture from a vendor's data book is generally an exercise in patience and pain. If you want to know more about the Pentium, however, there is a better way. Read *The Pentium Processor System Architecture* by Don Anderson and Tom Shanley. The 306-pg book presents a clear, concise, and well-written picture of the Intel Pentium architecture.

The book details the processor's implementation, helping you to understand the basic workings of the CPU, including the prefetcher, the two integer pipelines, and the floating-point unit. It also clarifies the intricacies of the caching mechanisms and memory-bus cycles. The authors describe the operations of multiple CPUs with secondary caches and the MESI (Modified Exclusive Shared Invalid) cache protocol. The book also includes several diagrams that supplement the text and make it easy to follow the descriptions and memory sequences.

The \$29.95 publication is part of a 5-book series on PC architectures. The series also includes books on the ISA, EISA, 80486, and PCI architectures.

—Ray Weiss

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MSM33S	Mixed supply voltage Usable density	2.7 ~ 3.6 V 4.5 ~ 5.5 V Up to 135k gates
MSM92S	Supply voltage High-density macrocells	2.7 ~ 5.5 V ROMs, single- and dual-port RAMS



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CIRCLE NO. 93



## VHDL engine speeds simulation

One way to crank out higher VHDL (VHSIC Hardware Description Language) simulation speeds is to design a simulator that compiles directly into the computer's native code. Although the native-code-compiler approach is effective, it's just another version of the old method of hot-rodding software: If it doesn't run fast enough in a high-level language, write it in assembly language. The attendant problem is that every new workstation presents a serious porting challenge; native-code-simulator companies are effectively in the compiler business.

Vantage takes a different approach in its SpeedWave VHDL simulation engine, while maintaining the portability benefits of compiling the VHDL into C code. Instead of speeding the execution

of sequential code, which is the primary benefit of a native-code compiler, Vantage works on the simulation-model part of the problem.

VHDL uses a complete and complex signal representation. However, much of the user-written code makes only simple demands on the VHDL models. Using what the company calls Bi-Level Adaptive Signal Trees (BLAST), the software creates a 2-level signal representation. The representations are classified as compact or complete. The compiler chooses the appropriate model for use in the simulation. The compact model not only saves memory, but processes faster and lets the compiler use a variety of optimization techniques not possible with the complete signal representation.

Users of the current Vantage VHDL

simulator need to do nothing different to take advantage of the speed improvements. Other than SpeedWave's faster simulation, which the company claims is up to 2× faster than other VHDL simulators, the change is transparent. The simulation results are VHDL-1076 compliant and 100% compatible with the current Vantage VHDL simulation engine. The company has a suite of more than 10,000 test programs, which are accumulated both internally and from customers verifying the results of the new simulator.

SpeedWave is free to all Vantage-Spreadsheet customers covered under maintenance agreements. Prices start at \$30,000.—**Doug Conner**

*Vantage Analysis Systems, Fremont, CA. (510) 659-0901. Circle No. 459*

**VHDL compiler implements version 1992/B.** The Leda VHDL 0.3 System (LDS) compilation environment lets users analyze VHDL models. The system allows users to store and access models in a binary data format via an ANSI-C language procedural interface. The system includes a schema compiler, a browser, library management, and a switch between 1987 and 1992 VHDL versions. The system runs on a Sparc or RS6000 platform. \$1000 (runtime licence), \$30,000 (development licence). **LEDA**, Meylan, France. 7641-9243. **Circle No. 460**

**Test-synthesis tool supports integration of ASIC- and pc-board-level test.** The Test Assistant test-synthesis tool provides automatic generation of Boundary Scan Description Language (BSDL) descriptions. The tool automatically generates the appropriate boundary-scan control pattern with the internal-scan test patterns to create a complete, unified test-pattern set for test-program generation. Test Assistant starts at \$40,000 and is available now. **Compass Design Automation**, San Jose, CA. (408) 433-4880. **Circle No. 461**

**Software links Verilog designs to IMS testers.** Integrated Measurement Systems (IMS) and its parent company, Cadence, offer software tools to smooth the transition between design and test. IMSLink lets you transfer simulation patterns directly from a Verilog simu-

lation environment into an IMS XL or an ATS test station. The software also lets you set up test vector files without accessing a test station. Cadence's Simulation Test Language (STL) is a stimulus-generation tool that lets you specify pin timing in a tester-compatible manner. Using STL during design verification ensures that the resulting test patterns are compatible with the tester. Alternately, you can use STL to find and correct timing-compatibility problems before transferring your patterns to a tester. IMSLink costs \$15,000 and will be available in the first quarter of 1994. STL is available immediately and costs \$5000. **Integrated Measurement Systems Inc**, Beaverton, OR. (503) 626-7117. **Circle No. 462**

**Cadence Design Systems Inc**, San Jose, CA. (408) 943-1234. **Circle No. 463**

**Create multilayer pc-board prototypes.** The Multi-Proto software package lets you create multilayer pc boards using IBC, T-Tech, and LPKF engravers. The system uses etching to create pc boards with as many as eight layers and uses the engravers for through-hole drilling and routing the board outline. Multi-Proto costs \$29,995. **Direct Imaging Inc**, West Lebanon, NH. (603) 298-8383. **Circle No. 464**

**Spice library for RF devices offers more than 300 models.** Version 3.0 of the RF-device library includes models for more than 100 BJTs, MMICs, and

GaAs MOSFETs supplied by Hewlett-Packard and more than 95 models for BJTs supplied by Philips. The library contains more than 300 models, including PIN diodes and can be used with any Berkeley Spice-compatible simulator. The device library costs \$150. Updates from version 2.0 cost \$50. **Intusoft**, San Pedro, CA. (310) 833-0710. **Circle No. 465**

**Module supports IEEE WAVES standard.** The Out-Converter module supports the Waveform and Vector Exchange Specification (WAVES) IEEE Standard 1029.1-1991, which is the standard for VHDL-simulation stimulus and expected data response. The module lets you use the company's Test Development Series (TDS) software with WAVES and VHDL. The WAVES Out-Converter is available now and costs \$10,000. **TSSI**, Beaverton, OR. (503) 643-9281. **Circle No. 466**

**AutoCAD for Windows provides 2-D drawing capabilities.** The AutoSketch (Release 2) 2-D drawing program for Windows provides drawing files that are upwardly compatible with AutoCAD. AutoCAD LT for Windows offers extensive 2-D drawing capability plus the ability to extrude 2-D drawings into 3-D and to modify 3-D drawings from AutoCAD. The software uses the same file format as AutoCAD. AutoSketch, \$299; AutoCAD LT, \$495. **Autodesk Inc**, Sausalito, CA. (415) 322-2344. **Circle No. 467**



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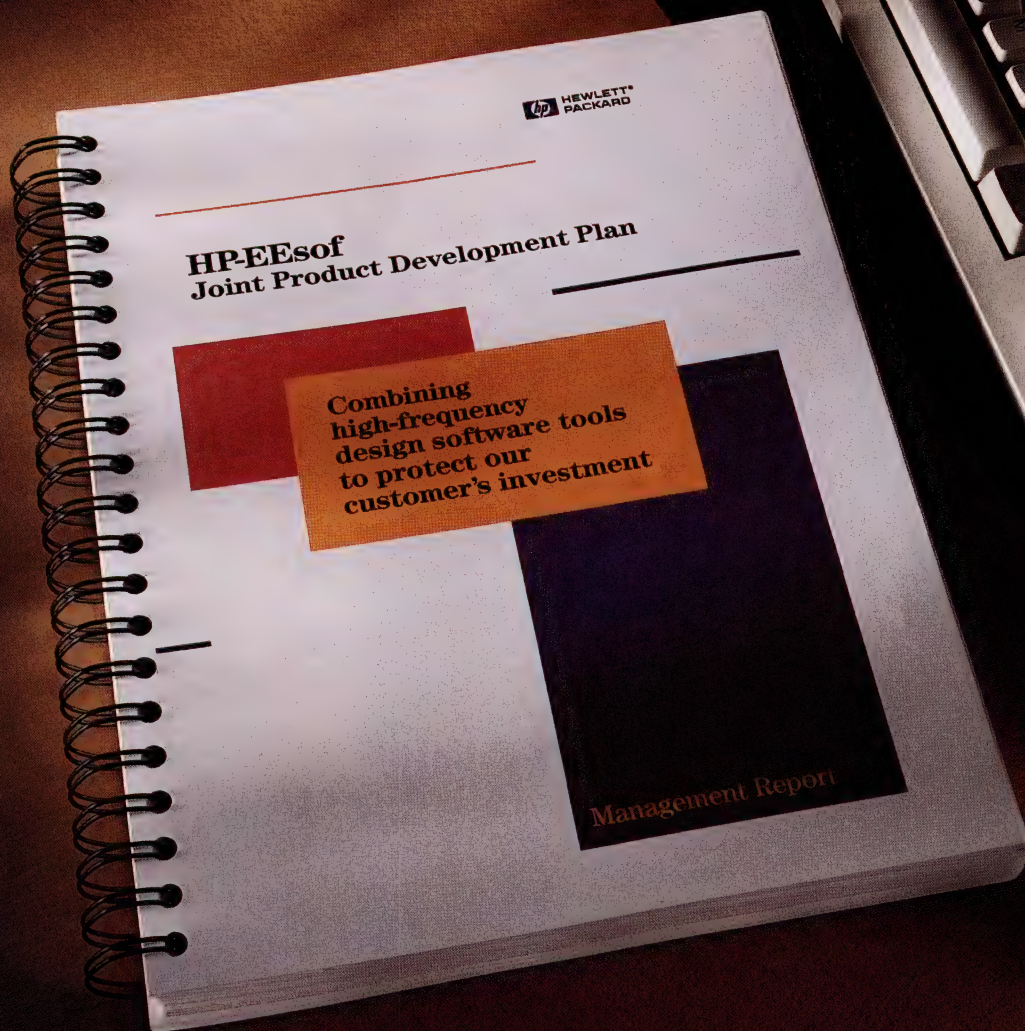
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## EDN-NEW PRODUCTS

### INTEGRATED CIRCUITS

# Power-factor correctors need few external components

In the next few years, US and European regulatory agencies will mandate that a broad range of products incorporate power-factor correction. The LT1248 and LT1249 power-factor controllers provide this correction for universal off-line power systems with very few external parts. For a wide range of loading conditions, the ICs achieve a power factor of over 0.99.

The ICs use fixed, high-frequency, PWM current averaging and require no slope compensation. The advantage of this approach is that the ICs achieve lower line-current distortion and can use lower-cost switches and magnetics than ICs or systems that rely on either

peak-current detection or zero-current switching.

To maintain low line-current distortion and high system stability with fewer external parts, the controllers use a multiplier that has a square gain function from the voltage amplifier and reduces the ac gain at light output loads. A low bias voltage at the multiplier's current input minimizes line-current dead zone.

The devices' numerous protection features include peak-current limiting and instantaneous overvoltage protection. The LT1248 can operate at frequencies as high as 300 kHz. The LT1249's switching frequency is fixed

at 100 kHz, but this IC comes in 8-pin DIPs (\$3.19) and SOICs (\$3.44); the LT1248 comes in 16-pin DIPs (\$3.53) and SOICs (\$3.76) (1000).

Typical startup supply current is 250  $\mu$ A; quiescent current is 9 mA. The devices include 1.5A peak-current gate drivers, which have a typical rise and fall time of 25 nsec. You can also synchronize the devices to an external signal frequency. The devices work with ac voltages from 90 to 270 and include line noise filters.—**Anne Watson Swager**

*Linear Technology Corp., Milpitas, CA. (408) 432-1900.* **Circle No. 380**

### Regulators suit battery-powered applications.

The REG1117-3, 3.3, and 5 are 3, 3.3, and 5V low-dropout voltage regulators that provide 800 mA of output current. A drop-in alternative to the LT1117, the devices operate down to 1V input-to-output differential, with a 1.2V max dropout voltage. On-chip trimming adjusts the reference/output voltage to within 1%. A trimmed current limit minimizes stress on the regulator and power-source circuitry under load conditions. Prices start at \$1.85 (1000). **Burr-Brown Corp.**, Tucson, AZ. (800) 548-6123. **Circle No. 381**

### IGBT features 1700V rating.

The MGxxxVxxx40 and xxx41 series IGBTs range in current from 30 to 360A and feature switching speeds of 0.4  $\mu$ sec. The devices feature a non-punch-through structure, which allows for 1700V blocking capability with square reverse-bias safe operating area and a better  $V_{CE(SAT)}$ -to-fall-time trade-off. The 180 and 360A packages for the higher-current devices reduce the inductance by 50%. The dual, 30A MG30V2YS40 module costs \$59.24 (one to 99). **Toshiba America Electronic Components Inc.**, Irvine, CA. (714) 455-2000. **Circle No. 382**

### Input controller mimics multiple keystrokes.

The Pilot EZ1000 input controller sends the equivalent of eight keystrokes to a DOS- or Windows-based computer for each transition of eight control switches. Intended for game controllers, the user-programma-

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ble device attaches to a 93C46 EEPROM and a PC game port. \$14.56 (100,000). **Rosetta Technology**, West Vancouver, BC, Canada. (604) 925-0820. **Circle No. 383**

### Video multiplexer integrates current-feedback amp.

The LT1204 4-input IC drives 150 $\Omega$  cables and operates on  $\pm 5$  to  $\pm 15$ V supplies. This multiplexer/amplifier provides channel separation and disable isolation >90 dB at 10 MHz. For large routing systems, you can parallel several LT1204s by shorting their outputs together to expand the number of inputs. The device features a -3-dB bandwidth of 75 MHz, gain flatness of 0.1 dB to 30 MHz, a 1000-V/ $\mu$ sec slew rate, and differential gain and phase of 0.04% and 0.06°, respectively. In 16-pin packages, prices for DIP and SOIC versions cost \$4.78 and \$5.20 (1000), respectively. **Linear Technology Corp.**, Milpitas, CA. (408) 432-1900. **Circle No. 384**

### Analog multiplexers extend signal range.

Four rail-to-rail multiplexer ICs handle signal levels out to the voltage-supply rails. The ADG4XX devices operate from  $\pm 15$  or single 5 to 12V and guarantee maximum 150-nsec break-before-make switching, 1.6-mW power consumption, typical 100 $\Omega$   $R_{ON}$ , and 5-pC charge injection. The 408 and 428—which start at \$3.50 (100)—switch between single-ended channels that you address using a 3-bit binary code. The 409 and 429—which start at \$3.15 (1000)—feature four differential input channels for noisy environments. The multiplexers guarantee operation in plastic packages over the extended industrial temperature range of -40 to +85°C. **Analog Devices**, Wilmington, MA. (617) 937-1428. **Circle No. 385**

### Single-chip video codec handles multiple algorithms.

The video controller processor (VCP) handles image compression and decompression, audio/video data demultiplexing, and image preprocessing and postprocessing. The image-processing functions include scaling, conversion between resolution formats, and picture-in-picture support. The programmable device handles JPEG, MPEG, and H.261 compression algorithms at clock rates to 66 MHz. \$140 to \$400 (1000), depending on speed grade. **Integrated Information Technology**, Santa Clara, CA. (408) 727-1885. **Circle No. 386**

**Analog switches improve  $R_{ON}$  matching.** The MAX301, 303, and 305 dual, precision ICs feature an on resis-



# EDN-New Products

## INTEGRATED CIRCUITS

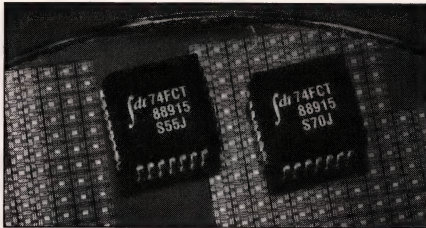
tance of  $35\Omega$  that remains flat to within  $\pm 3\Omega$  over the analog-signal range. The on resistances in each device match to within  $\pm 2\Omega$ . The switches feature leakages of  $<250$  pA at  $25^\circ\text{C}$  and  $<6$  nA at  $85^\circ\text{C}$ . Turn-on and -off times are  $<150$  and  $100$  nsec, respectively. The switches can operate with a  $10$  to  $30\text{V}$  supply or with dual supplies of  $\pm 4.5$  to  $\pm 15\text{V}$ . In  $20$ -pin PLCCs,  $16$ -pin DIPs, and narrow SO packages, prices start at  $\$1.23$  for the 301 and  $\$2.57$  for the 303 and 305 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 387**

**Graphics accelerator has  $1280 \times 1024 \times 24$ -bit resolution.** The North-Star VRAM-based graphics accelerator provides  $1280 \times 1024 \times 24$ -bit/pixel noninterlaced resolution. The  $64$ -bit chip provides  $16$ -,  $24$ -, and  $32$ -bit color modes, which allow photorealistic displays. The CL-GD5452 has an integrated dual-clock synthesizer that produces the pixel clock, which is programmable to  $135$  MHz. A memory clock is programmable to  $60$  MHz. A  $32$ -bit direct-connect host bus connects to a PCI or VL local bus. A companion CL-GD5453 IC is a  $135$ -MHz,  $24$ -bit, dedicated, paletted DAC. Chip set,  $\$65$  (1000). **Cirrus Logic Inc**, Fremont, CA. (510) 623 8300. **Circle No. 388**

**Core logic gives Pentium multiprocessing capabilities.** The Hydra chip set for the Pentium  $\mu\text{P}$  supports the symmetrical multiprocessing features of Windows NT and Unix. Four chips integrate as many as four CPUs onto the  $64$ -bit-wide multiprocessor-interconnect (MPI) bus. The chips comprise a CPU controller, a bus controller, and two memory-interface chips. The HT354 CPU controller provides the gateway between the Pentium processor and the MPI bus and provides secondary cache control. The HT352 bus-control unit bridges the MPI bus to a local peripheral-component-interconnect (PCI) bus. The HT355 ECC and data-pipeline chip provide error correction for the memory subsystem. HT354,  $\$265$ ; HT352,  $\$190$ ; HT355,  $\$65$ . **LSI Logic Corp**, Milpitas, CA. (408) 433-8000. **Circle No. 389**

**Serial EEPROMs have 32-kbit capacity.** The 24C32 and 24LC32 serial EEPROMs have  $32$ -kbit capacity without having to cascade devices. The device exceeds the requirements of the I<sup>2</sup>C specification, a 2-wire bus defining

$16$  kbits as the maximum serial address space. It extends the I<sup>2</sup> bus protocol from 1 byte to 2 bytes and implements functional address-select lines.  $5\text{V}$  24C32,  $\$3.17$ ;  $2.5\text{V}$  24LC32,  $\$3.49$ . **Microchip Technology Inc**, Chandler, AZ. (602) 786-7200. **Circle No. 390**



**Clock-driver chip employs PLL.** The IDT54/74FCT88915 clock-driver chip uses a CMOS phase-locked loop (PLL) to provide a zero delay between clock generation and distribution. The output skew is specified as  $500$  psec, and the device is pin-, form-, and function compatible with Motorola's 88915 clock-driver IC. The chip produces eight outputs at a maximum frequency of  $133$  MHz. You can use any of the outputs as a feedback reference for the PLL. A reference-select pin controls a two-to-one input multiplexer to select either of two synchronous sources. A frequency-select pin provides additional divide-by-two control of the output frequency.  $\$9$  (1000). **Integrated Device Technology Inc**, Santa Clara, CA. (800) 345-7015. **Circle No. 391**

**Error-correction IC encodes and decodes HDTV signals.** The AHA 4011 codec provides Reed-Solomon forward error correction for high-speed digital data streams. The chip provides on-the-fly correction at a continuous data-transfer rate of  $10$  Mbytes/sec for block lengths of  $54$  to  $177$  bytes and a clock rate of  $40$  MHz. A burst-mode operation corrects all block lengths at  $40$  Mbytes/sec. The device can also operate in pass-through mode.  $\$30$  (1000). **Advanced Hardware Architectures**, Moscow, ID. (208) 883-8000. **Circle No. 392**

**NAND flash memory provides 16 Mbits of storage.** The KM29N16000T flash-memory device uses NAND gates instead of the traditional NOR gates, providing more memory density than the traditional configuration. Other features include  $5\text{V}$  operation,  $1$  million endurance cycles,  $15$ - $\mu\text{sec}$  random-access read time,  $80$ -nsec sequential page-access time,  $300$ - $\mu\text{sec}$  automatic page-program time,  $6$ -msec automatic

block-erase time, and  $10$ -year data retention.  $\$98$  (100). **Samsung Semiconductor Inc**, San Jose, CA. (408) 954-7274. **Circle No. 393**

**Flash memory fits in BIOS EPROM socket.** The DiskOnChip nonvolatile flash-memory chip offers as much as  $16$  Mbits of storage that fits into a standard PC BIOS socket. Using the chip in handheld computers provides a bootable storage device that extends battery life. The device uses the embedded flash-file system to emulate the organization and management of a standard generic read/write disk device. The chip has a data-transfer rate of  $50$  Mbps and operates from  $5\text{V}$ .  $1$ -Mbit version,  $\$99$  (100). **Eurom**, Fremont, CA. (510) 505-9083. **Circle No. 394**

**Comparators resolve 2-mV signals without oscillating.** The MAX915/916 single/dual TTL-compatible, edge-triggered comparators have a master/slave architecture that enables them to resolve small input voltages over the common-mode range. The ICs' propagation delay is  $6$  nsec, and the delay is insensitive to input overdrive, whether the overdrive is  $3$  mV or  $1\text{V}$ . Because the input common-mode range extends to the negative supply rail, the ICs suit  $5\text{V}$  ground-sensing applications. The ICs operate from either a dual  $\pm 5\text{V}$  or a single  $5$  to  $10\text{V}$  supply. Each comparator consumes  $70$  mW.  $1000$ -piece prices start at  $\$2.55$  for the 915 and  $\$3.90$  for the 916. **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 395**

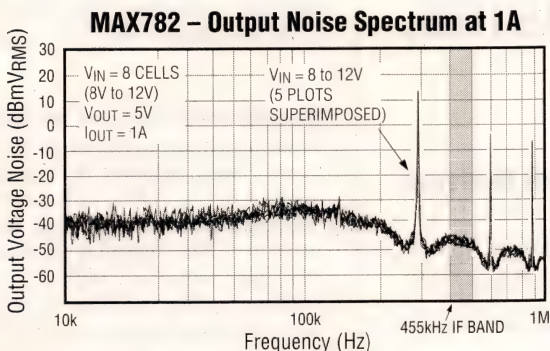
**MOSFET keeps low profile.** The MIC94001BLM p-channel MOSFET has a low  $8$ -pin height of  $0.063$  in. The  $0.006$ -in. difference from similar p-channel devices allows this device to fit the low-overhead section of PCMCIA hard-disk-drive designs. The MOSFET features a maximum on resistance of  $0.40\Omega$  and operates with gate-threshold voltages as low as  $0.8\text{V}$ . Rated for the extended industrial-temperature range of  $-40$  to  $+125^\circ\text{C}$ , the device costs  $\$1.05$  (1000). **Micrel Semiconductor Inc**, San Jose, CA. (408) 944-0800. **Circle No. 396**

**3.3V SRAM has 70-nsec access time.** The  $256$ -kbit HM62W256 SRAM operates from  $3.3\text{V}$  and provides a  $70$ -nsec access time. The CMOS device acts as cache or buffer memory in hard-disk drives and portable battery-pow-

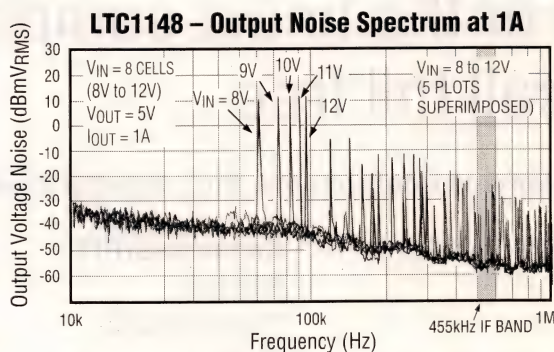


# STOP INTERFERENCE CAUSED BY YOUR NOTEBOOK POWER SUPPLY

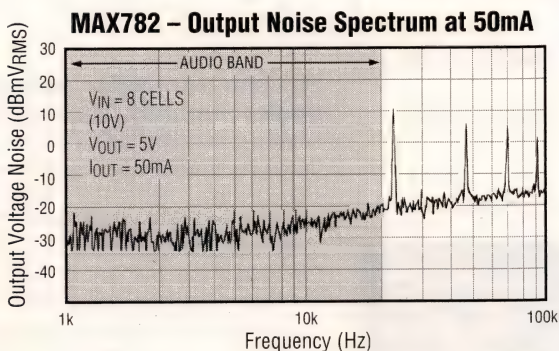
Power controllers use Idle Mode™ architecture, which is more than 30dB quieter than Burst Mode™ in the critical audio and IF bands



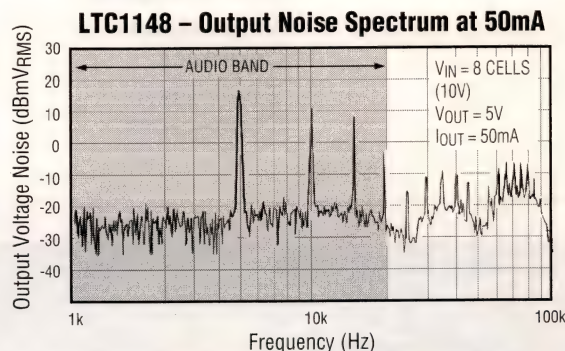
The MAX782's output is clean, stable and quiet at 1A load currents – only the 300kHz fundamental and simple harmonics are present. No noise is generated in either the audio or 455kHz IF band.



The LTC1148 changes frequency as the battery or AC adapter voltage changes, so noise is scattered across a broad band of the spectrum – including the sensitive 455kHz IF region.



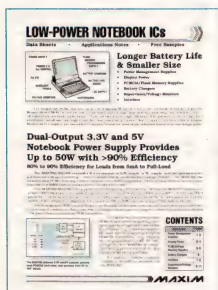
With light loads, the MAX782 operates in Idle-Mode™ and stays well above the audio range. Even with only a 50mA load, the MAX782 still operates above 20kHz, which is excellent for multi-media PCs.



Burst-Mode™ noise dominates the audio range when the LTC1148 operates at the same 50mA load. The result is very difficult to filter, and this is a significant source of interference in these noise-sensitive systems.

Maxim has the most complete family of power controller ICs for notebook computers, offering the world's highest performance and efficiencies to 96%. The MAX782/MAX783 support 2 PCMCIA slots and have 3.3V, 5V and 15V outputs, while the MAX786 has 3.3V and 5V outputs. And for Power PC™ designs, all three parts offer a 3.6V output option. To speed your design, Maxim offers preassembled, tested evaluation kits.

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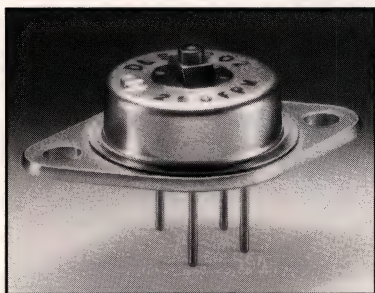
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## EDN-NEW PRODUCTS

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ered systems. The chip has a 32k×8-bit organization and comes in a 32-pin TSOP or 26-pin SOJ package. The device draws 27 mA while operating, and dissipation in standby mode is 0.66  $\mu$ W. Center  $V_{CC}$  and  $V_{SS}$  pins reduce I/O noise. SOJ version, \$6.25 (1000). **Hitachi America Ltd**, Brisbane, CA. (415) 589-8300. **Circle No. 397**

#### Sound card shrinks to single chip.

Packing the equivalent of the Creative Labs Sound Blaster audio card into a single IC, the ES1488 handles 8-bit monaural sound. The chip, which operates at 3.3V, includes audio-compression and music-synthesis circuits. A related device, the ES688, offers stereo audio without music synthesis for Windows Sound System applications. Both devices cost <\$20 (10,000) and are sampling now. **ESS Technology Inc**, Fremont, CA. (510) 226-1088. **Circle No. 398**

#### Efficient controller powers notebook computers.

The MAX786 power-supply controller includes separate step-down regulators for 3.3 and 5V. The IC also includes separate comparators for low-battery backup and two low-dropout, micropower linear regulators for supplying backup power to CMOS RAM and real-time clocks. Efficiency for the 3.3 and 5V supplies is as high as 95% for 2A loads and greater than 80% for loads from 3 mA to 3A. The IC's input range is 5.5 to 30V. The 420- $\mu$ A quiescent current drops to 70  $\mu$ A in the standby mode and to 25  $\mu$ A in the shutdown mode. The 200- or 300-kHz operating frequency of the current-mode PWM-architecture IC allows it to operate with small external components. The device comes in a 28-pin SSOP package; prices start at \$4.15 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600. **Circle No. 399**

#### Dot-clock IC has dual PLLs.

The ICS2572 dot-clock IC provides a PECL-compatible output at 185 MHz. Two on-chip PLLs provide a memory output and a video differential output. Because it can switch frequencies on the fly without BIOS calls, the chip is compatible with Windows NT and suits high-end video applications. It lets you redefine the frequency selection after power-up, which permits the setup of a frequency table on initialization. It provides 16 video and four memory locations, which are reprogrammable via a serial input. \$5.50. **Integrated Circuit Systems Inc**, Valley Forge, PA. (215) 630-5300. **Circle No. 400**

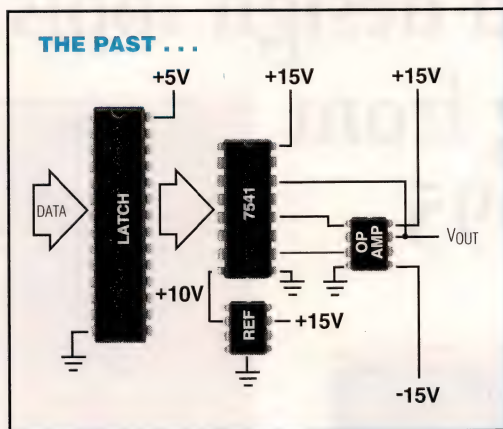


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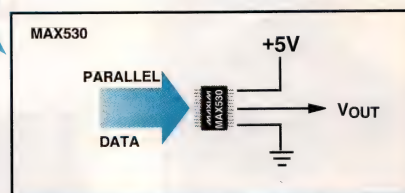
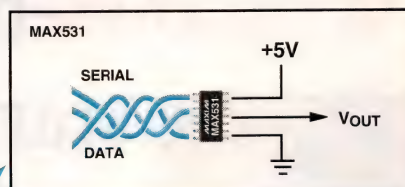
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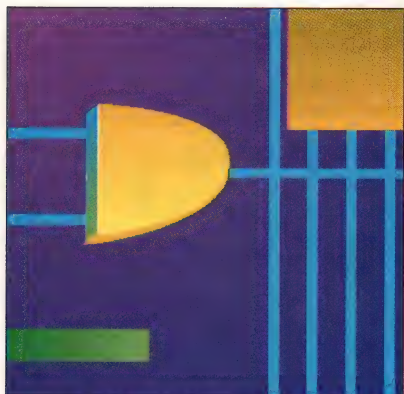
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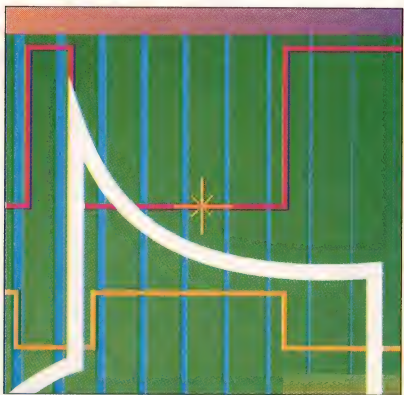
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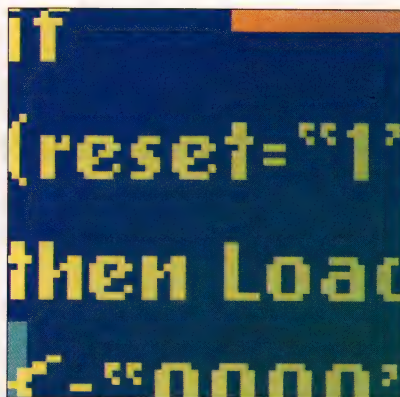
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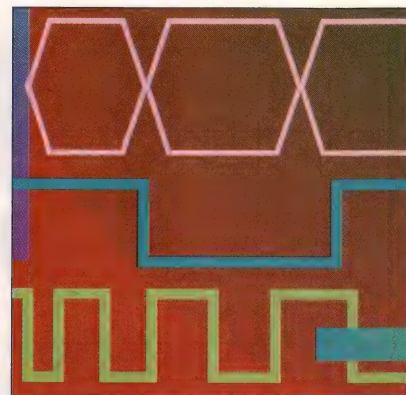
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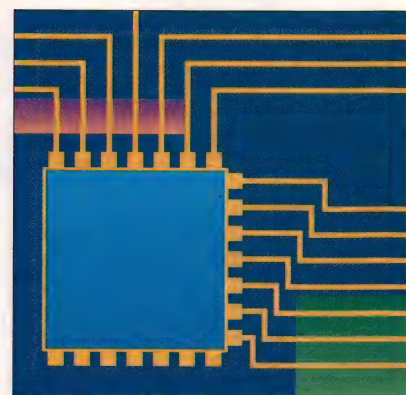
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## ADC/DAC/DSP instrument offers high resolution, low noise, high speed

Sonitech's DAQ-200 is not your father's ADC. Nevertheless, in some ways, it evokes the ADCs of a generation ago. Like the high-performance converters of that day (yes, they did exist), it mounts outside its host computer. While this approach is more expensive than building a data-acquisition unit on an I/O card, the cost isn't prohibitive, and the benefits are great: The much quieter environment outside the computer results in excellent S/N ratios. And because the unit contains its own intelligence—a 33-Mflop TMS320C31 DSP (optionally two) with up to 4 Mbytes of zero-wait-state SRAM—you can sometimes dispense with the host. A dumb device, such as a parallel-interfaced handheld terminal, can provide the control.

The DAQ-200 costs \$2495. Its 5.45×1.52×12-in. aluminum enclosure provides shielding on all sides and houses two sampling, 18-bit, 200k-sample/sec ADCs that sample simultaneously and two 20-bit DACs. The ADCs and DACs are spec'd to 16 bits. Optical isolators couple all digital signals into and out of the converters. Panel-mounted switches allow easy experimentation with the analog-power-supply and shield "ground" connections to minimize noise. The unit includes a 6.4-Mbps C30 serial port and a 24-line parallel interface. Power comes from an



**Shielding on all sides, optical isolation of digital signals, and an external linear power supply are three features that enable Sonitech's DAQ-200 to deliver 16-bit THD on two channels digitized simultaneously at 200k samples/sec. The unit also contains two high-resolution DACs, a 33-Mflops DSP, and up to 4 Mbytes of zero-wait-state SRAM.**

externally mounted low-noise linear supply.

Sonitech measures the THD and noise performance of each channel of every unit and ships printouts of those measurements to customers. Unipolar and bipolar full-scale ranges are software programmable in four steps from 0.1 to 10V for the ADCs and in three steps from 1 to 10V for the DACs. You can plug in linear antialiasing filters to limit the bandwidth of the analog signals applied to the ADCs, and you can bypass these filters under software control.

Although delta-sigma ADCs are becoming increasingly popular in audio applications, the DAQ-200 uses successive-approximation ADCs. There are two main reasons why: First, you can't buy 16-bit delta-sigma ADCs that make 200k conversions/sec; second, in closed-loop-control applications, the pipeline delay through delta-sigma converters often causes intractable stability problems.

—Dan Strassberg

Sonitech International Inc, Wellesley, MA. (617) 235-6824. **Circle No. 413**

**Handheld DMMs provide 3½ or 3% digits.** The DM-311 through DM-335 handheld DMMs are protected to 600V in the resistance, continuity, and diode-check modes. They withstand 1000V between common and ground. A mechanical gate disables the 10A input jack until the user selects the proper range. The units emit a pulsed audible warning if the test leads do not correspond with the function selected. Prices for 3½-digit models begin at \$49.95; 3%-digit units start at \$69.95. **GoldStar Precision Co Ltd**, Cerritos, CA. (310) 404-0101.

**Circle No. 414**

**Drivers enable control of microwave instruments from LabWindows for DOS.** Software drivers for the vendor's 360B vector network

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analyzer, 5400A series and 562 scalar network analyzers, 6700B-series swept-frequency synthesizers, and 68100A-series synthesized sweep generators work with National Instruments' LabWindows for MS-DOS. The drivers provide function-panel interfaces that automatically generate the correct instrument command codes and syntax. These codes become part of the C or Basic source code of your instrument-control program. \$700 to \$1795. **Wiltron Co**, Morgan Hill, CA. (408) 778-2000.

**Circle No. 415**

**\$119 handheld 4½-digit DMM resolves 10 µV, 0.1 µA, and 0.01Ω.** The 380551, which receives power from a 9V battery, offers basic dc accuracy within 0.05%. A rotary switch selects the unit's ranges and functions. A shock-absorbing holster is standard; a padded vinyl pouch costs \$15. **Extech Instruments Corp**, Waltham, MA. (617) 890-7440.

**Circle No. 416**

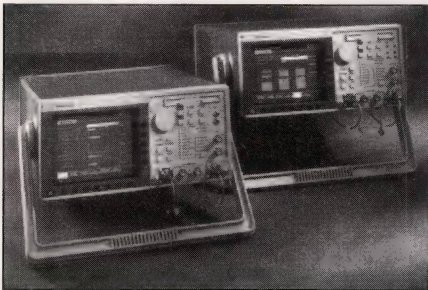
**In-circuit component tester uses 64-channel, 25-MHz state machine for triggering.** The Testmate 3064's internal high-speed modeling circuit supports more than 600 standard IC types. When testing LSI ICs, the system compares the unit under test against a user-supplied known-good device. The tester makes pass-fail decisions and provides details about



# EDN-NEW PRODUCTS

## TEST & MEASUREMENT

each IC pin, such as signal frequency and whether the pin is stuck, toggling, or floating. \$9995; 28-channel version \$6995. **ZTest Electronics Inc.**, Buffalo, NY. (416) 238-3543. **Circle No. 417**



**Test sets automate SDH and SONET field testing.** The CTS 710 (for SONET) and the CTS 750 (for SDH) perform comprehensive monitoring and transmission testing. They also offer byte manipulation for troubleshooting and analysis. The units adapt to changing requirements via software upgrades that you can install through a built-in floppy-disk drive and via signal-interface plug-ins. The standard plug-in handles electrical inputs and outputs to 155 Mbps. An optional interface provides electrical and optical inputs and outputs to 622 Mbps. Either test set costs \$15,900. **Tektronix Inc.**, Beaverton, OR. (800) 426-2200. **Circle No. 418**

**Numeric-solution software runs under MS-DOS.** Speakeasy for PC-DOS performs array and matrix algebra and statistical analysis; solves linear, quadratic, and differential equations; and lets you create graphics interactively. The underlying routines are time-tested; mainframe and workstation versions have been available for years. The \$995 package requires at least an 80386 CPU with math coprocessor, 6 Mbytes of RAM (8 Mbytes recommended), and 10 Mbytes of hard-disk space. **Speakeasy Computing Corp.**, Chicago, IL. (312) 427-2400. **Circle No. 419**

**3.6-GHz vector network analyzers measure 0.5 msec/point.** With their 10 markers, the Advantest R3762AH and R3765B automatically calculate and display such parameters as center frequency, bandwidth, dB down, Q, and shape factor. The units, which detect zero-phase frequencies without your having to move a marker away from the measurement point, let you rapidly determine the frequencies at which the phase differs from zero by

a programmable amount. By including controllers that offer serial, parallel, and IEEE-488 ports, the instruments obviate the need for host computers. From \$24,000. **Tektronix Inc.**, Beaverton, OR. (800) 426-2200. **Circle No. 420**

**BSDL translator lets you use Asset debugger to view control cells.** BSM2HSM converts Boundary-Scan Description Language files to Hierarchical-Scan Description Language (HSDL). With the HSDL format, you can use the Scan-View feature of Texas Instruments' Asset debugger to view control cells that otherwise are not observable. \$295. **Intellitech Corp.**, Meredith, NH. (603) 279-6308. **Circle No. 421**

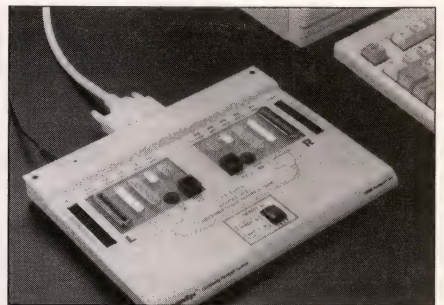
**Portable instrumentation recorder uses standard VHS cassettes.** The 24-channel StorePlus VL records voice, digital, and analog data. All analog channels have a bandwidth of 100 kHz at all times. Their dynamic range is 55 dB. You can substitute 600-kbps digital channels for analog channels in any combination. Help displays permit quick access to such features as a real-time clock/calendar/timer and track sequencing for extended recording and replay. With eight channels, the 11.5×17.5×9-in. system weighs 33 lb and costs \$16,200. **Racal Recorders Inc.**, Irvine, CA. (714) 727-3444. **Circle No. 422**

**AC-line-dip and interrupt-test modules meet IEC 1000-4-11.** The EP61, EP62, and EP64 test modules work with the vendor's ECAT series of pulsed-EMI test systems. Besides testing for susceptibility to line interruptions and voltage dips, the modules test for overvoltages, or "swells." The EP61 tests at 125V/20A and 250V/16A, the EP62 tests at 250V/32A, and the EP64 works with 3-phase equipment at 250V/32A from each phase to ground. From \$26,540. **KeyTek Instrument Corp.**, Wilmington, MA. (508) 658-0880. **Circle No. 423**

**Synthesized 1-μHz to 1.1-MHz sine-wave source offers -65-dBc harmonic distortion to 20 kHz.** The Model 98 oscillator uses direct digital synthesis. You can set its output frequency with 8-digit precision and <30-ppm error. The generator can synchronize with a 10-MHz reference that you supply. With a 50Ω load, the 50Ω output adjusts from 15 mV to 15V p-p (30 mV to 30V p-p with a high-impedance load). A 600Ω, 30-Hz to

200-kHz transformer-coupled output adjusts from 15 mV to 30V p-p across 600Ω. The front-panel display can indicate the output level in peak, peak-peak, or rms volts or dBm. The generator offers fully programmable logarithmic and linear sweeps. \$2795; delivery 6 weeks, ARO. **Wavetek Corp.**, San Diego, CA. (619) 279-2200. **Circle No. 424**

**<\$3000/pin digital-IC test system handles 200-MHz data rates.** The ATS Blazer! system tests complex, high-speed devices at high throughput rates. You can also configure the system to test mixed-signal devices. You can upgrade the pin count to 832 pins in 16-channel increments. A 125-MHz version costs approximately \$2500/pin. You can upgrade systems in the ATS family to Blazer! performance. **Integrated Measurement Systems Inc.**, Beaverton, OR. (503) 626-7117. **Circle No. 425**



**PC-based cable tester presents graphic wiring displays.** The 701 CableEye system includes an annotated cable database to which users can add. The system displays wiring diagrams on screen in color and produces labels and wiring diagrams on laser and dot-matrix printers. The test fixture, which handles additional connector types via extender boards, connects to a PC's serial port. Menu-driven software performs functions that the vendor claims are not available on any other system. \$1495. **CAMI Research Inc.**, Lexington, MA. (617) 860-9137. **Circle No. 426**

**Unit programs and verifies 32 1-Mbyte flash cards in 13 sec.** The CardServer-32X extension of the vendor's Proteus-GMC16 memory-card tester reads, writes, tests, and exercises PCMCIA V2.0/JEIDA V4.1 type I, II, and III devices, such as modems, fax modems, and rotating-memory cards. The unit operates in a stand-alone mode or on a network. \$9950 to \$19,950. **B&C Microsystems Inc.**, Sunnyvale, CA. (408) 730-5511. **Circle No. 427**





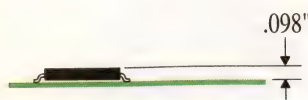
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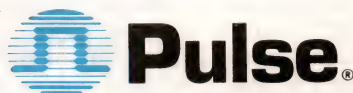
Complete interface magnetics modules contain filters, isolation transformers, common-mode chokes and resistor networks, all designed to match IBM, TI, NSC, and other interface chips. Transmit & receive all in one package only 1.25" x .735" x .098".

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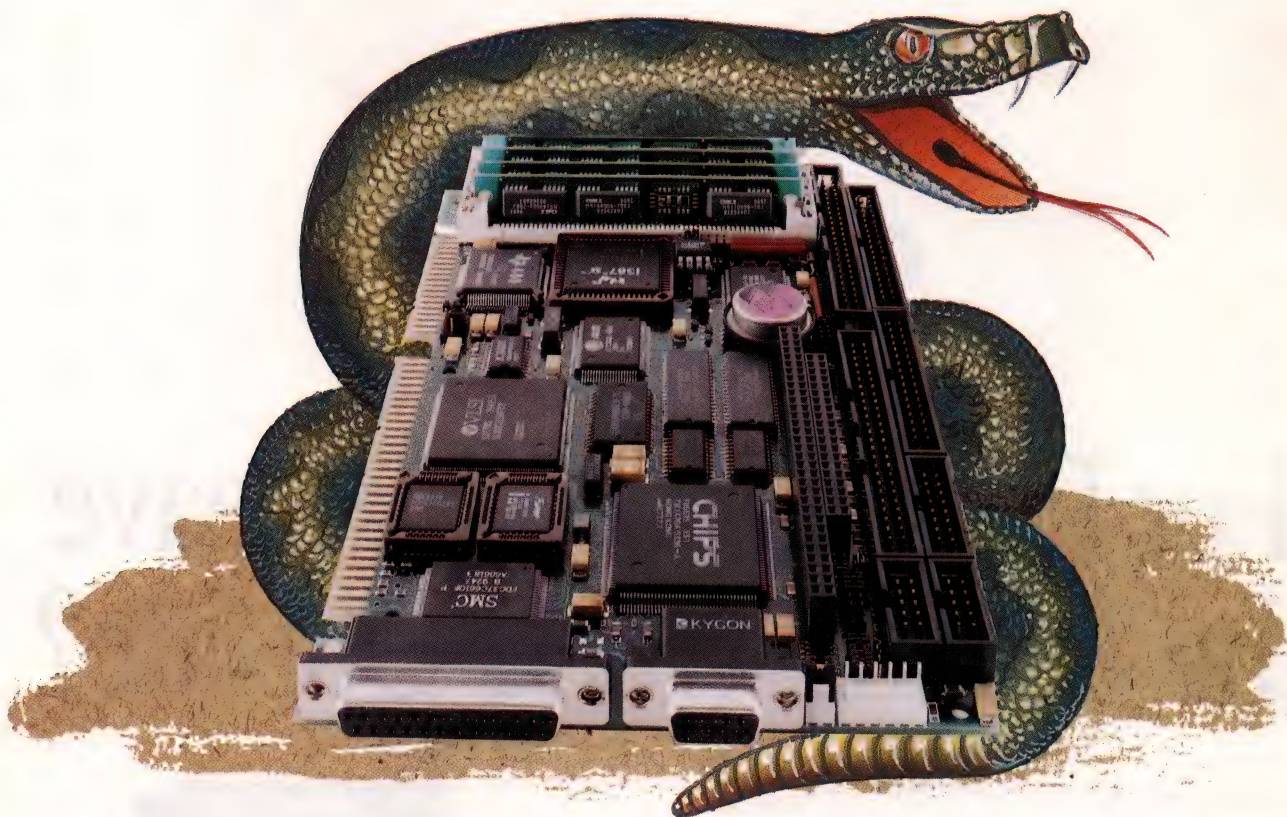
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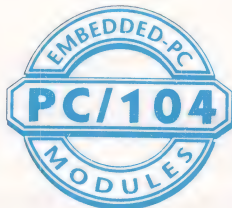


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## POWER SOURCES

**Miniature 8W dc/dc converters are 100% burned in.** The 800 series of 8W dc/dc converters is 100% burned in for 72 hours. The units' 6-sided metal case measures 1×2×0.375 in. They operate over a -30 to +71°C range with no derating or heat sinking. The series features 5, 12, and 15V outputs in single-, double-, and triple-output models. The units also have input filters and remote on/off control. \$58 to \$66.50. **Conversion Devices**, Brockton, MA. (508) 559-0880. **Circle No. 401**



**Distributed-power 75W converters are programmable.** The MicroMod dc/dc converters have programmable output voltages and current limits. The units' 6-sided metal cases measure 1.5×1.8×0.5 in. and handle 75W. Depending on model, input voltages range from 5 to 300V, and output voltages range from 3.3 to 24V. All units feature output trim and remote sense. You can parallel these converters without interconnecting a control line. Efficiency is 80% typ. \$50 to \$70. **Power Micro Inc**, Chelmsford, MA. (508) 250-0400. **Circle No. 402**

**Off-line switchers accommodate 88 to 264V-ac inputs.** The NFS line of off-line switching supplies operates from US and European power lines. The family comprises 25, 40, 50, 75, 110, 200, and 350W models. The supplies' manufacturing plant is ISO 9000 registered, and the supplies meet UL, CSA, VDE, and BABT/BSI safety specs. Medical versions meet UL544 and IEC601 standards, and others meet FCC and VDE Class B line-conducted emission limits. \$24 to \$220. **Computer Products Inc**, South Boston, MA. (617) 268-1170. **Circle No. 403**

**Front end configures itself for 120 or 230V ac.** The UNV-300 is an ac/dc "front end" for 300V-input power supplies. The device senses the line voltage and configures itself for 120 or 230V ac operation. The unit handles 700W over a -40 to +75°C range without derating. Efficiency is 97% at full power. \$130. **Powercube Corp**, Billerica, MA. (508) 667-9500. **Circle No. 404**

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**Low-cost supplies correct power factor.** The PGC series of multiple-output power supplies meets IEC 555-2 requirements for power-factor correction. The series is available in 300, 500, 750, and 1000W models featuring three, four, or five outputs. The supplies' outputs are independently regulated, requiring no preload. The units measure 2.65 in. high. \$475. **Lambda Electronics Inc**, Melville, NY. (516) 694-4200. **Circle No. 405**

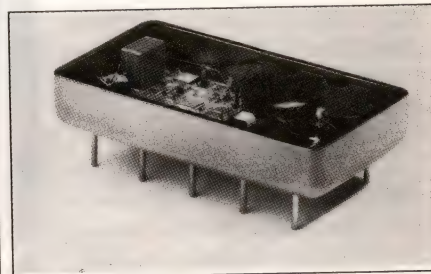
**Low-cost lab supply has triple outputs.** The HP E3630A triple-output dc power supply's main output ranges from 0 to 6V at 1 to 2.5A max. The 0 to -20V outputs provide 0.5A max. Normal-mode noise specs are 0.35 mV max, and common-mode current is 1  $\mu$ A max. The supply features digital meters and a single voltage control for both secondary supplies. All outputs have overload and short-circuit protection. \$500. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844, ext 7941. **Circle No. 406**

**Linear supply powers transducers.** The model CM1.10.400 ruggedized 10V linear supply powers 14 350 $\Omega$  transducers. The unit features screw terminals for field wiring. The supply's voltage accuracy is  $\pm 1\%$ , and noise and ripple measure 1 mV rms. Line and load regulation is  $\pm 1\%$ , and the temperature coefficient is 0.01%/°C. \$120.75 (1 to 5). **Calex Mfg Co Inc**, Concord, CA. (510) 687-4411. **Circle No. 407**

**DC/DC converters feature choice of input ranges.** The M and K families of 50 and 150W supplies offer 20 to 100, 28 to 14, and 44 to 220V dc inputs. Universal ac inputs are also available. The units operate over -25 to +71°C. Single and dual outputs up to 48V dc are standard. Triple-output M models are also available. M family: \$426; K family: \$689 (25). **Melcher Inc**, Chelmsford, MA. (508) 256-1812. **Circle No. 408**

**Modular 400W supply lets you mix and match outputs.** The model M400 modular, open-frame switching supply offers a standard switchable or an optional automatic 115/230V ac

input. The supply carries a main 5V dc at 50A main output and as many as three auxiliary outputs. Auxiliary outputs can be 5 to 12V at 10A, 12 to 24V at 5A, or  $\pm 12/15$ V at 1A. The unit measures 2.5×5×12.5 in. and is UL, CSA, and VDE listed. FCC Class B filtering is standard. \$0.85/watt. **Xentek Inc**, San Marcos, CA. (619) 471-4001. **Circle No. 409**



**MIL-STD 20W converters baby their power transistors.** The OHD2800S series of single-ended forward converters handles 20W over the military temperature range. Outputs are 5, 12, or 15V; inputs range from 16 to 40V. These fixed-frequency converters use a resonant-transformer reset circuit, which allows their output transistors a maximum 67% duty cycle. You can synchronize the units at 425 or 525 kHz. Efficiency is 81%. The units meet NAVMAT P-4855-1A and MIL-STE-704D. \$325 (100). **Omnirel Corp**, Leominster, MA. (508) 534-5776. **Circle No. 410**

**External supplies have universal input.** This 8-model line of 25W external power supplies feature a universal input of 90 to 265V ac. The units have outputs of 5, 9, 12, 15, 16, 24; 5 and 12; and 5 and  $\pm 12$ V. All units are foldback and short-circuit protected and are approved to UL1950, CSA 22.2 No 223, TUV EN60950, and IEC950. \$30 (OEM). **Ault Inc**, Minneapolis, MN. (612) 493-1900. **Circle No. 411**

**DIP converters output 1W.** D-3 dc/dc converters output 1.2W (1W for the 5V output models). Housed in a DIP-type package measuring 0.5×0.4 in., the units accept inputs of 5, 12, 15, or 24V and output 5, 9, 12, 15, 24,  $\pm 5$ ,  $\pm 12$ , or  $\pm 15$ V. Output voltage accuracy equals  $\pm 5\%$  and total output ripple and noise measures 150 mV p-p max. Operating range spans 0 to 70°C. \$18.75 and \$19.75 for single- and dual-output models, respectively. **Alban Inc**, Santa Clara, CA. (408) 988-3949. **Circle No. 412**



## PCMCIA flash-memory cards provide storage options

Two new PCMCIA cards from Intel give you flash-memory storage with a choice of system-implementation methods. The series 2+ PCMCIA flash card works with flash-file-system (FFS) software; the PCMCIA-ATA drive emulates an IDE disk drive. The FFS-compatible card comes in 4-, 20-, and 40-Mbyte versions; the ATA card has capacities of 5 and 10 Mbytes.

The FFS card automatically configures for 5 or 3.3V operation; the ATA card operates on 5V. Both cards have internal voltage converters that provide 12V for write operations. Ran-



**New PCMCIA flash cards from Intel come in two versions. Those shown here work with flash-file-system (FFS) software; others emulate an IDE disk drive.**

dom-access reads occur in 150 nsec (with 5V operation) on the FFS card; seek time on the ATA card is <1 msec. Write speeds are 850 and 220 kbytes/sec on the FFS and ATA cards, respectively.

The FFS card provides 64-kbyte software-lockable memory blocks. The ATA card's controller provides wear leveling, error detection and correction, file management, and power management. FFS card, \$220 to \$1895 (1000); ATA card, \$310 and \$475 (1000).—Gary Legg

*Intel Corp., Santa Clara, CA.  
(800) 879-4683. Circle No. 428*

**PCMCIA system connects to PC bus.** The PCMCID, a PCMCIA-interface system, comprises a half-size PC-bus interface module, a 1- or 2-slot card drive, and a cable. The drive, which will accept Type I, II, or III cards, can be as much as 18 in. away from the PC-bus backplane electronics. It has the dimensions of a 3.5-in. floppy-disk drive and can mount in a regular drive bay. The interface module provides BIOS support for autoboot memory cards. 2-drive system, \$290 (OEM). **Computer Dynamics**, Greer, SC. (803) 877-8700. **Circle No. 429**

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**PCMCIA card adds RS-232C port.** The RS-232C adapter is a PCMCIA Type II card with an industry-standard 9-pin connector for RS-232C operation. It operates at rates as high as 115.2 kbps and comes with floppy disks containing diagnostic and configuration software. \$145 (1000). **IBM Microelectronics**, Hopewell Junction, NY. (800) 426-0181. **Circle No. 431**

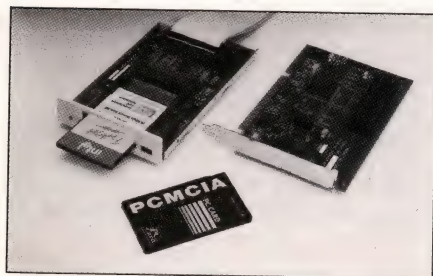
**Card contains PCMCIA-to-SCSI adapter.** Visual Media SCSI is a Type I PCMCIA card that allows the use of SCSI peripherals with portable PCs. It comes with software that allows easy installation of devices without using jumpers. The device lets you daisy-chain as many as seven SCSI devices. \$339. **New Media Corp.**, Irvine, CA. (714) 453-0100. **Circle No. 432**

**Removable disk cartridge stores 270 Mbytes.** The SQ3270 is a 3.5-in., 270-Mbyte removable-cartridge disk drive that is backward compatible with SyQuest's 105-Mbyte cartridge system. The drive has an AT/IDE interface and features 13.5-msec access time. Cartridges cost about \$80; drive with one cartridge, \$465. **SyQuest Technology**, Fremont, CA. (510) 226-4000. **Circle No. 433**

**Modem has 230.4-kbps throughput.** The Optima 288 V.FC + Fax external modem provides data-throughput rates of 28.8 kbps (with compression). The modem supports V.Fast Class (V.FC), ITU-T (formerly CCITT) V.42 bis data compression, ITU-T V.42 error control, and Group 3 fax using V.17. It's compatible with V.32 bis, V.32, and V.22 bis modems. \$579. **Hayes Microcomputer Products Inc.**, Norcross, GA. (404) 840-9200. **Circle No. 434**

**Touch frame fits flat-panel displays.** The Modular/1LP, a low-profile IR touchscreen for flat-panel displays, fits 200×150-mm displays from Hitachi, Panasonic, Sharp, and Toshiba. Programmable amplification makes the unit impervious to most severe ambient-light conditions. The unit is available with a PC/104 or an RS-232C controller. \$380. **Carroll Touch**, Round Rock, TX. (512) 244-3500. **Circle No. 435**

**PCMCIA drive has internal and external versions.** CardPro 2 adds two PCMCIA slots to a PC; it's available both as an external unit and in a version for mounting in a computer's 3.5-in. drive bay. The slots accept Type I, II, and III cards, plus the thicker, 18-mm cards that are as yet officially unsanctioned by PCMCIA. Interface to the drive is via a card that plugs into the PC bus. \$350. **Data I/O Corp.**, Redmond, WA. (800) 332-8246. **Circle No. 436**



**PCMCIA drive installs in PCs.** The Enable PCMCIA device controllers, which allow the use of PCMCIA cards in desktop computers, support Intel's ExCA specification and allow hot insertion and removal of cards. Each system comprises a half-length AT-bus card, a cable, and a PCMCIA socket assembly, which mounts in a PC's drive bay. EnableOne, with one socket, costs \$295; EnableTwo, with two sockets, is \$350. **MSD3**, Morgan Hill, CA. (408) 778-7267. **Circle No. 430**



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AK2351F	•	•	•		•	1.9~5.5	2400 bps MSK MODEM
AK2352	•	•	•	•		1.9~5.5	2400 bps MSK MODEM
AK2353	•	•	•	•	•	1.9~5.5	2400 bps MSK MODEM
AK2354	•	•	•	•	•	1.9~5.5	1200 bps MSK MODEM
AK2359	•	•	•	•	•	1.9~5.5	FSK MODEM
AK2356				•		2.6~3.3	SCRAMBLER ONLY

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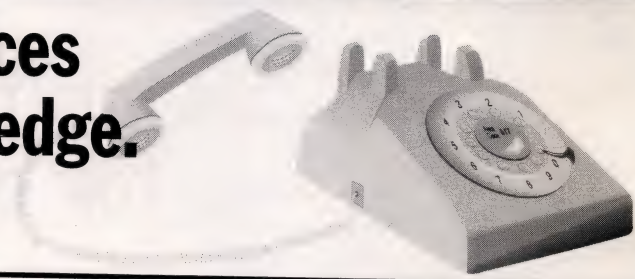
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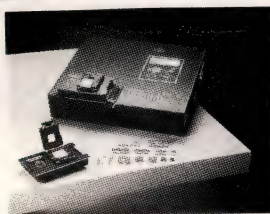
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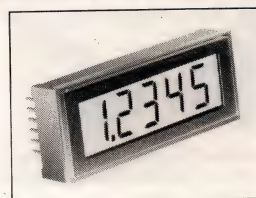
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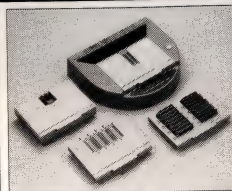
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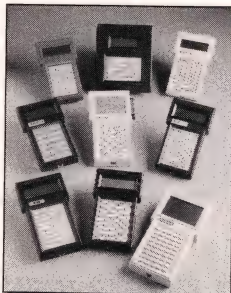
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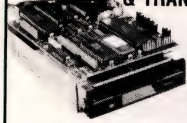
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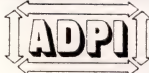


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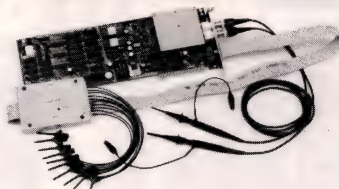


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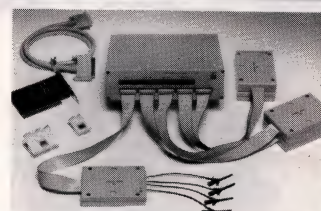


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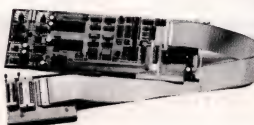
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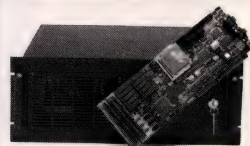
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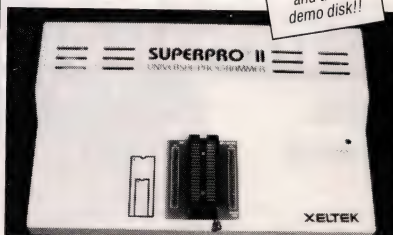
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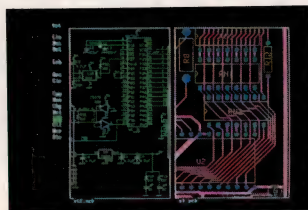
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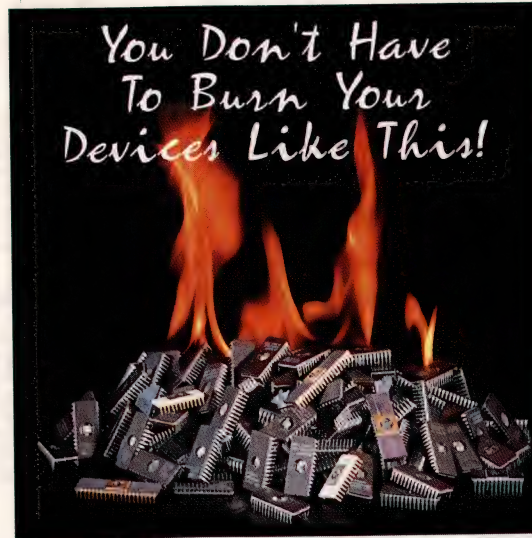
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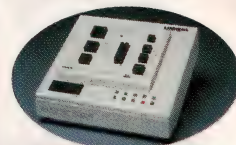
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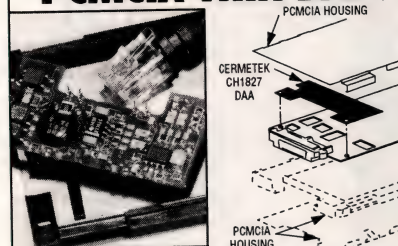
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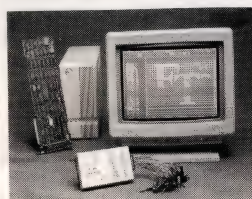
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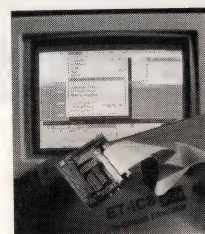
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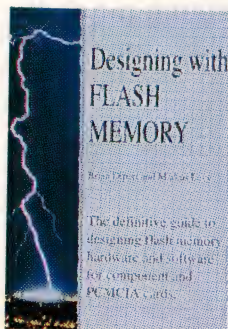
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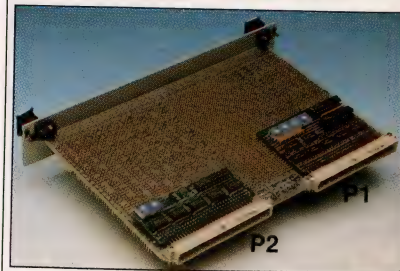
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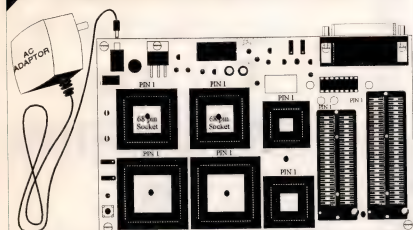
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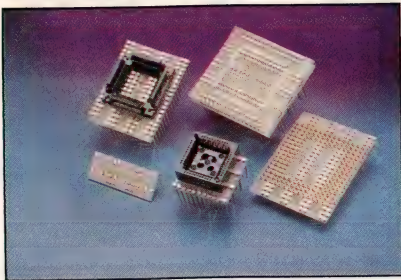
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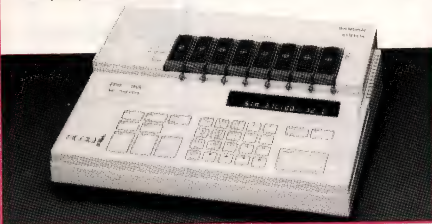
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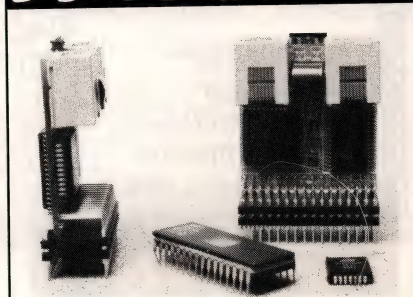
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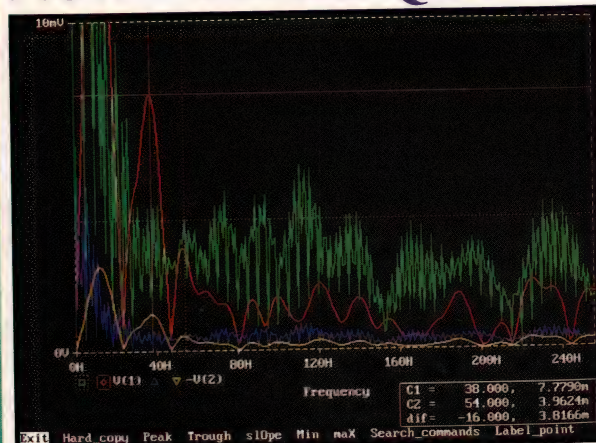
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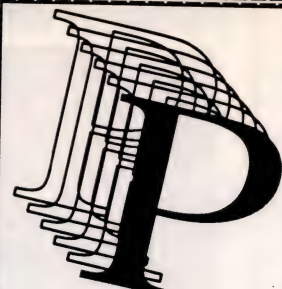
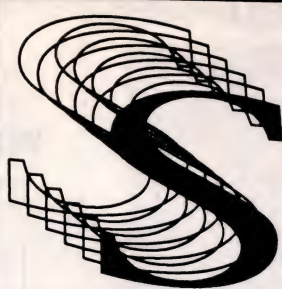
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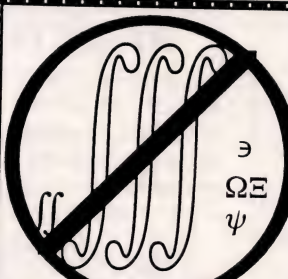
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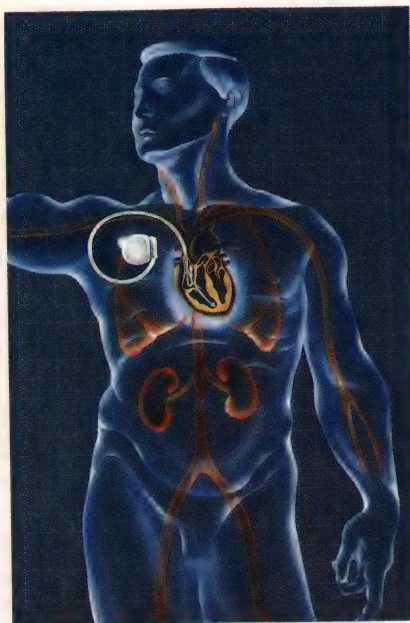
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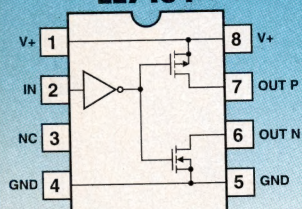
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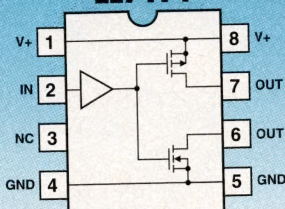
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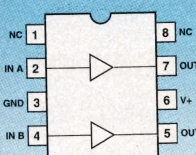


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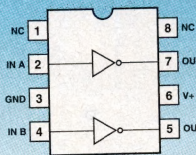
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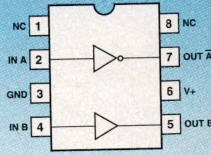
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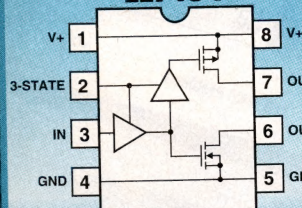


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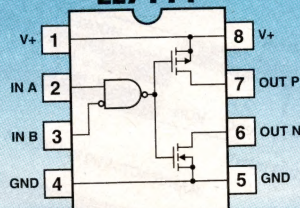
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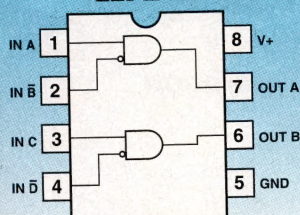
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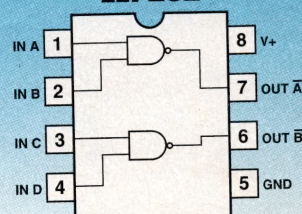
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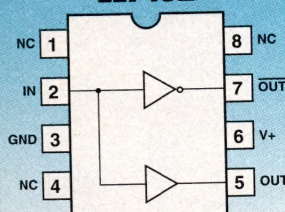
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- \$2.25 - 100's P-DIP

**EL7252**



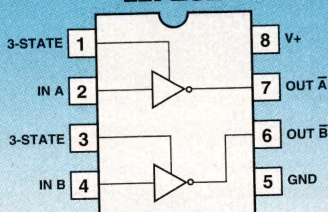
- 20 ns Prop Delay
- 20 ns Switching Time
- \$2.25 - 100's P-DIP

**CCD Driver/Dual Channel 3-State Line Driver  
EL7182**



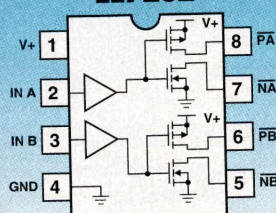
- Reduced Clock Skew
- 20 ns Switching Time
- \$2.65 - 100's P-DIP

**EL7232**



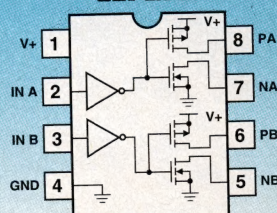
- 20 ns Prop Delay
- 20 ns Switching Time
- \$2.25 - 100's P-DIP

**Dual Channel - Isolated Drains, 2.0 Amps  
EL7262**



- 20 ns Prop Delay
- 20 ns Switching Time
- \$2.25 - 100's P-DIP

**EL7272**



- 20 ns Prop Delay
- 20 ns Switching Time
- \$2.25 - 100's P-DIP

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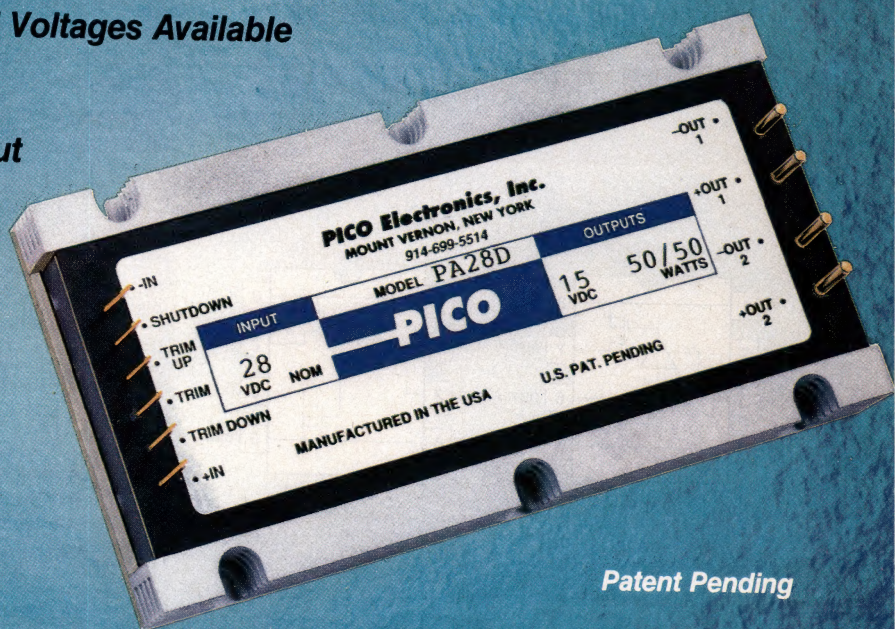
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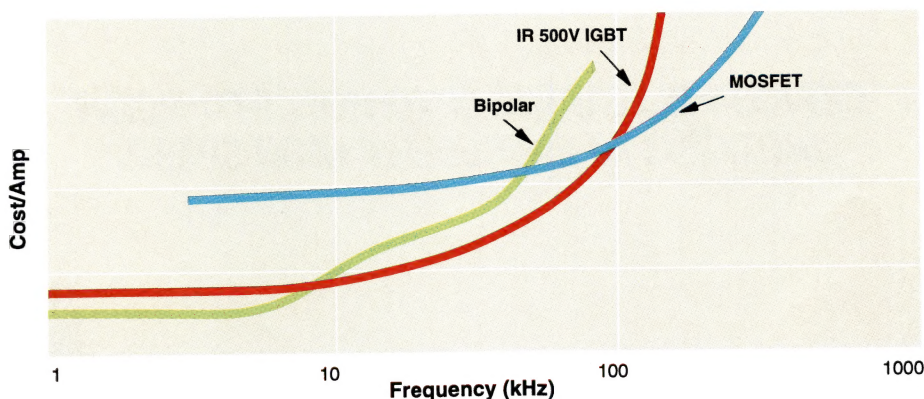
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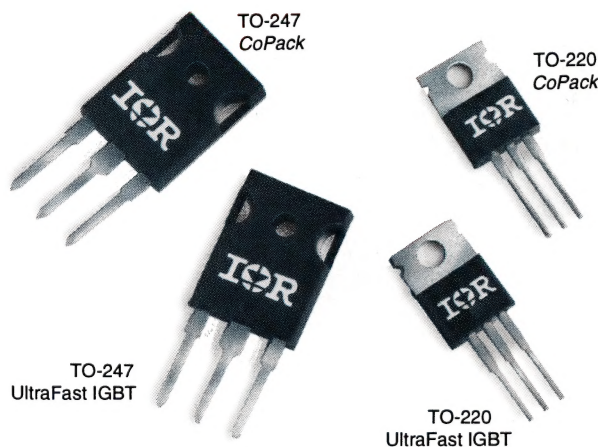


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